Major Assignment Final Term Summer

Course Name: Digital Logic Design

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BS (SE-8) Section: A

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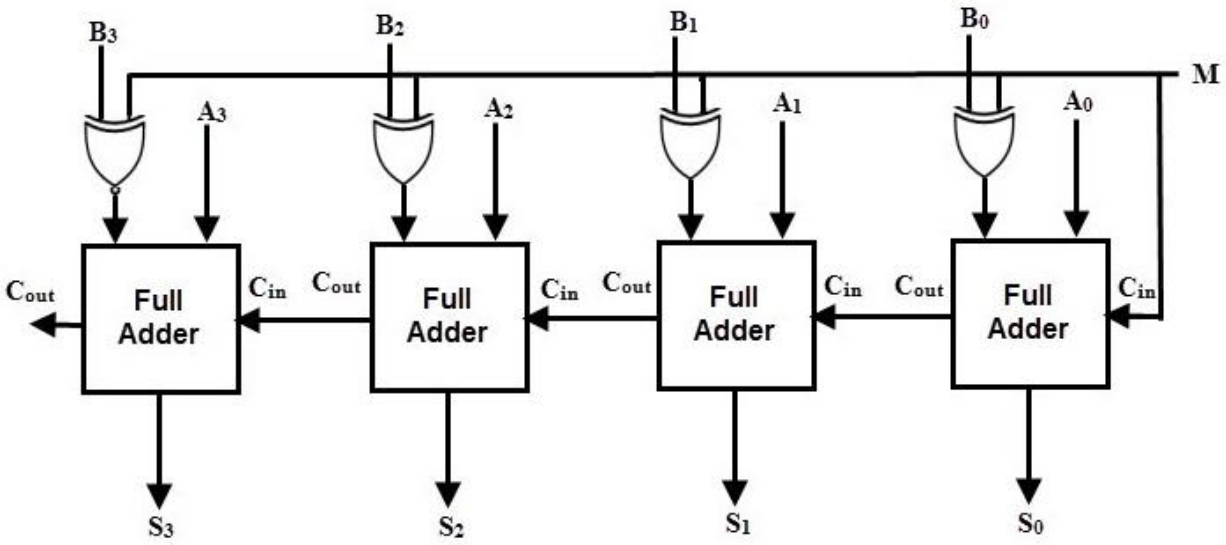
Q1 (a)

Answer:

Circuit Diagram



Explanation:

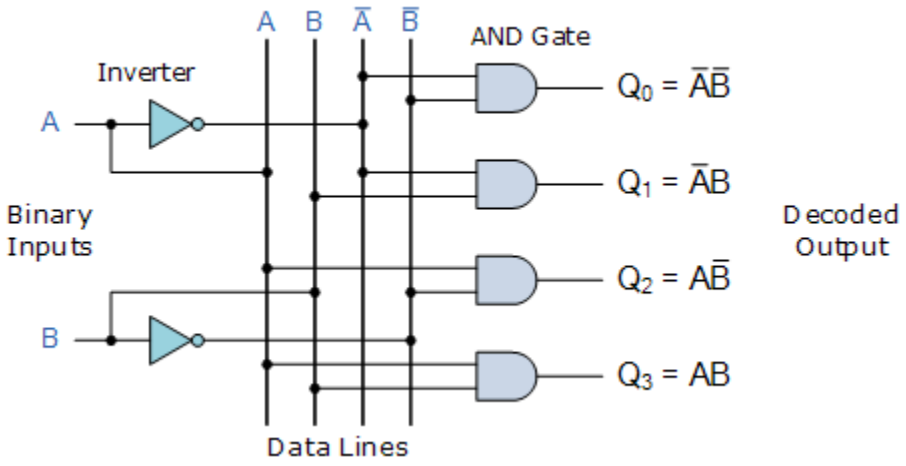
When M= 1, the circuit is a subtractor and when M=0, the circuit becomes adder. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When M = 0, B Ex-OR of 0 produce B. Then full adders add the B with A with carry input zero and hence an addition operation is performed.

When M = 1, B Ex-OR of 0 produce B complement and also carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.

Q1 (b)

Answer:

Decoder



Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Explanation:

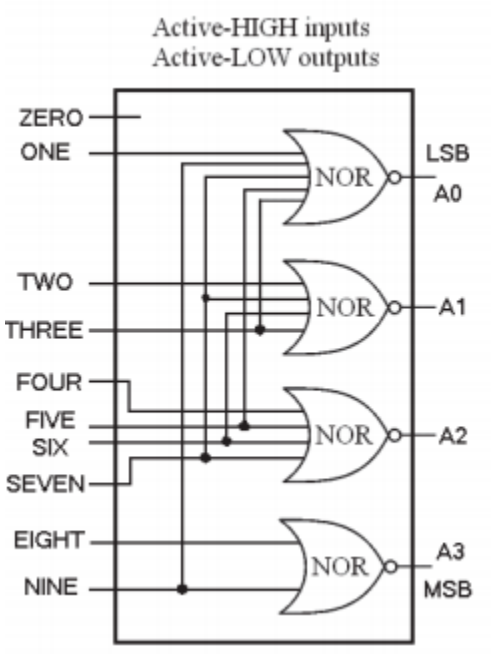
This simple example above of a 2-to-4 line binary decoder consists of an array of four AND gates. The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the miniterms of the 2 input variables, (each output = a miniterm).

The binary inputs A and B determine which output line from Q0 to Q3 is “HIGH” at logic level “1” while the remaining outputs are held “LOW” at logic “0” so only one output can be active (HIGH) at any one time. Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “de-codes” the binary input.

Q1 (c)

Answer:

Decimal to BCD Encoder



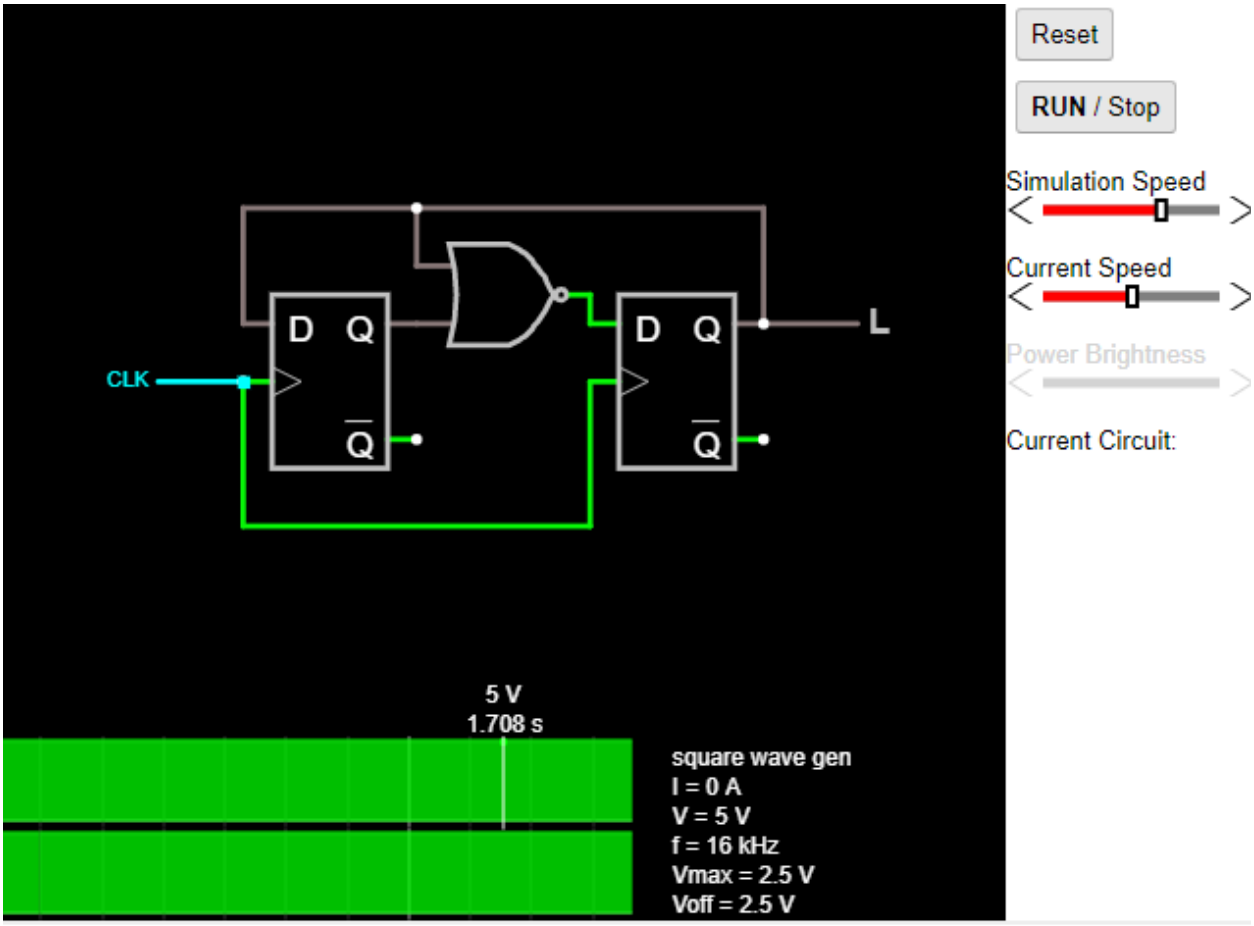
Explanation:

A decimal-to-BCD encoder is a digital circuit that has 10 input lines and 4 output lines. The inputs represent the 10 decimal numbers from 0 to 9, where only one input can be active. The outputs indicate the BCD code that represents the active input. Above circuit shows the logic diagrams of the decimal-to-BCD encoder using NOR gates. For the case of active-H i/ps and active-L o/ps, the logic diagram with NOR gates is used. By adding a SE inverter at the end of each output, one can get active-H o/ps. It can be noted that the encoder needs 1 NOR gate with 2 inputs (which is connected to the MSB output), 1 NOR gate with 5 inputs (which is connected to the LSB output), and 2 NOR gates with 4 inputs (which are connected to the middle two outputs).

Q1 (d)

Answer:

Frequency Divider



This circuit shows how two D flip-flops can be used to divide the frequency of a clock signal by 3.

Q2

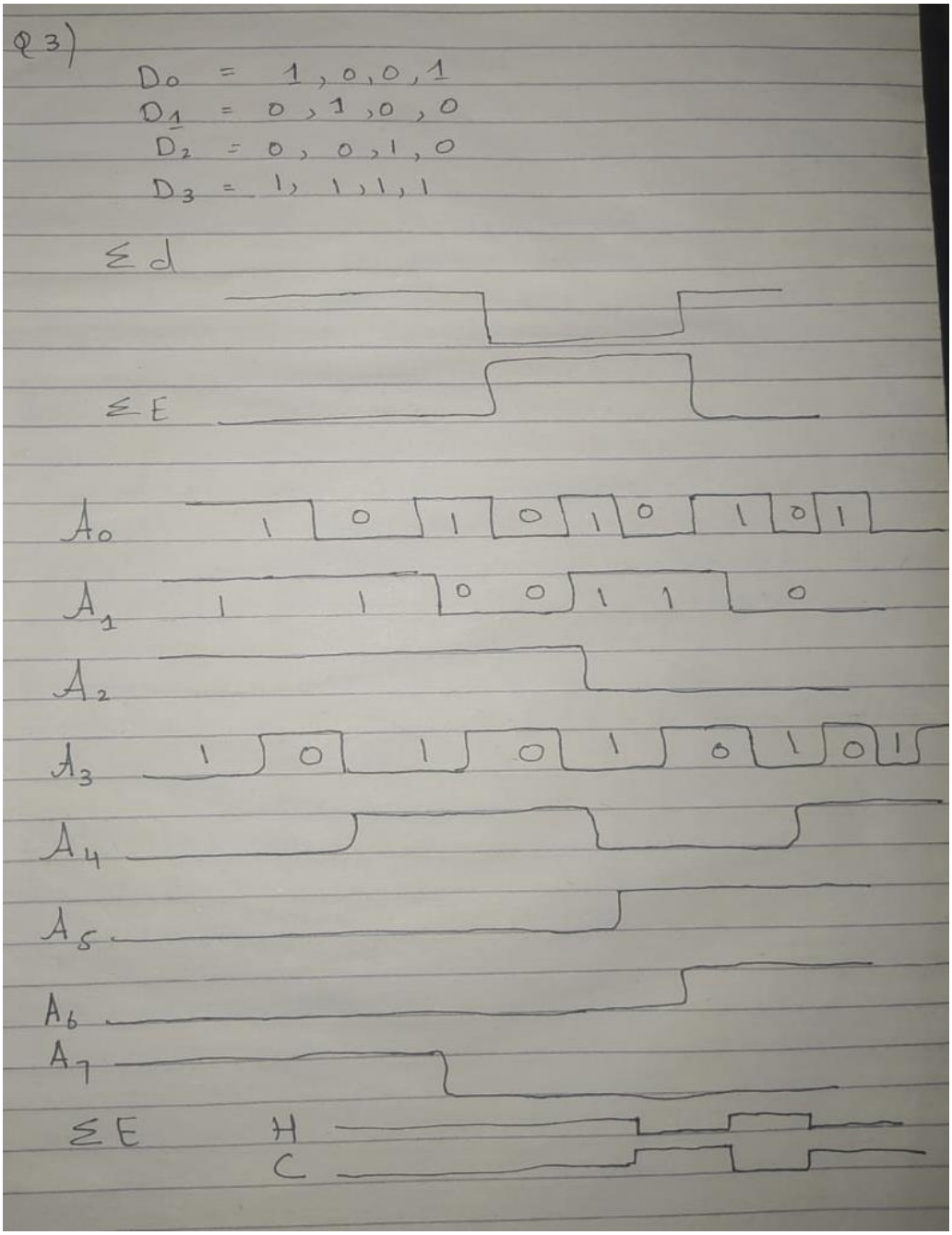
Answer:

The truth table of a 4-to-1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D0, D2, D1 and D3 to the output. That means when S1=0 and S0 =0, the output at Y is D0, similarly Y is D1 if the select inputs S1=0 and S0= 1 and so on.

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Q3

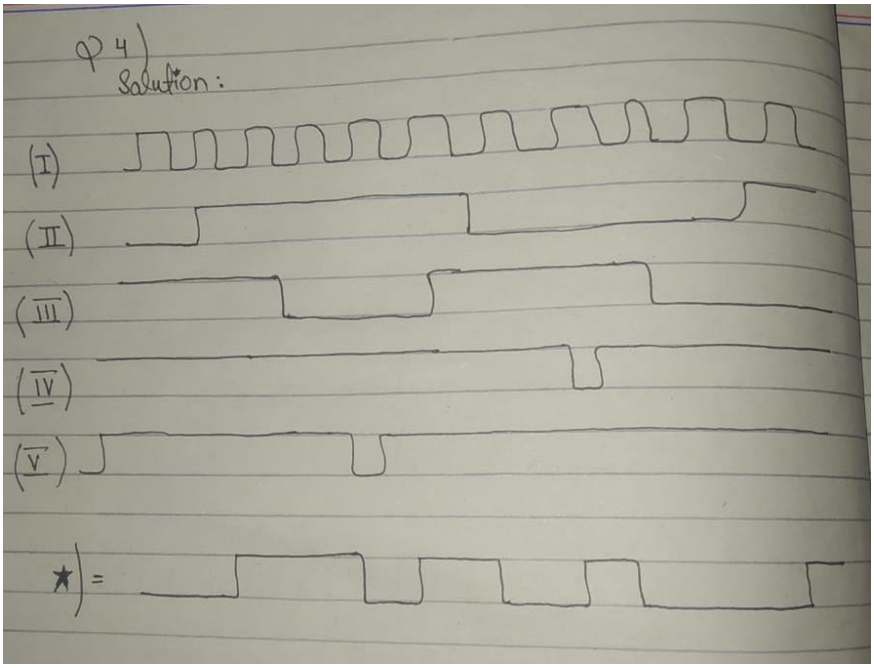
Answer:


Q3)
D0 = 1, 0, 0, 1
D1 = 0, 1, 0, 0
D2 = 0, 0, 1, 0
D3 = 1, 1, 1, 1
Ed
EE
A0
A1
A2
A3
A4
A5
A6
A7
EE
H
C

Q4

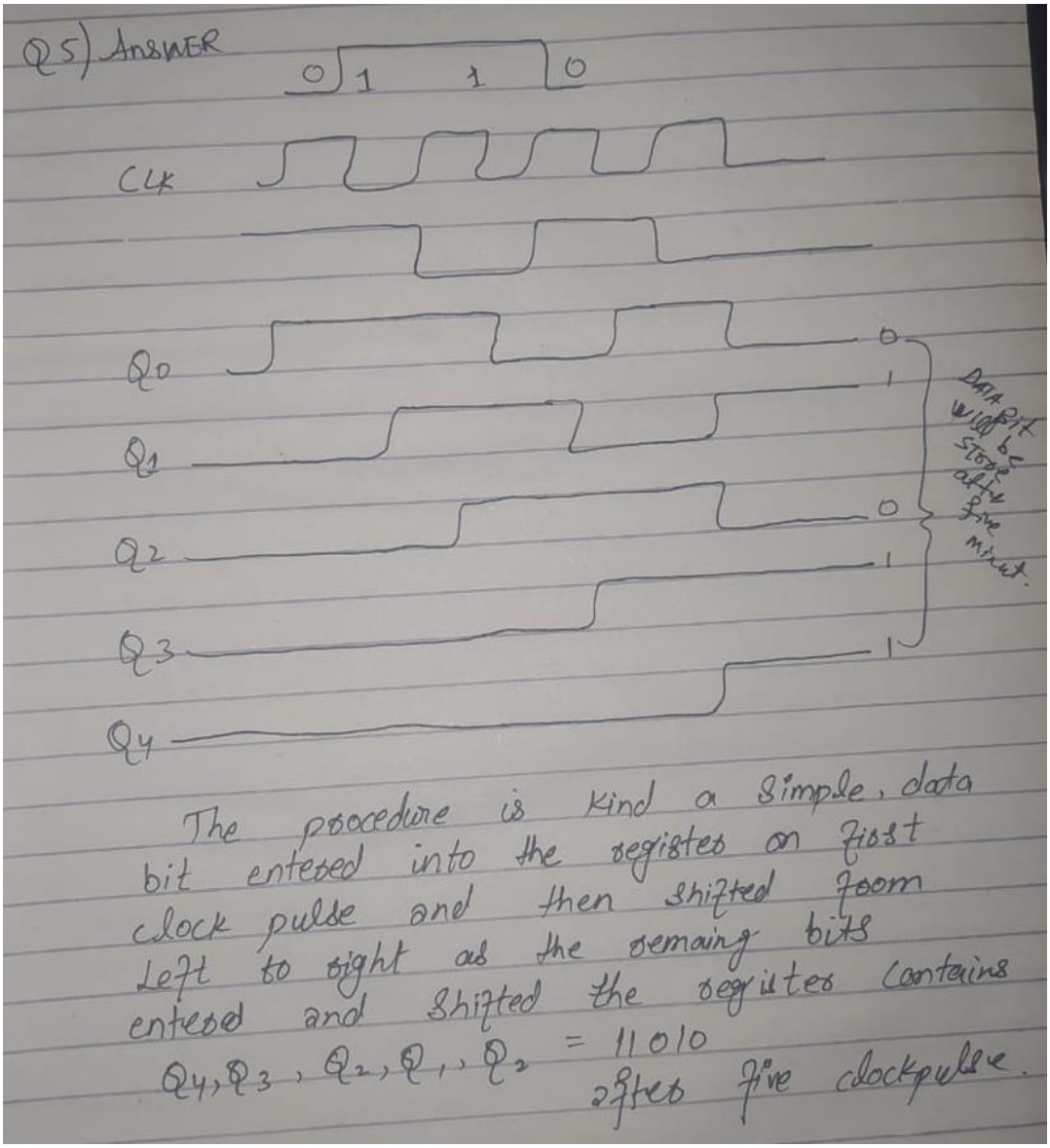
Answer:

Q Output:



Q5

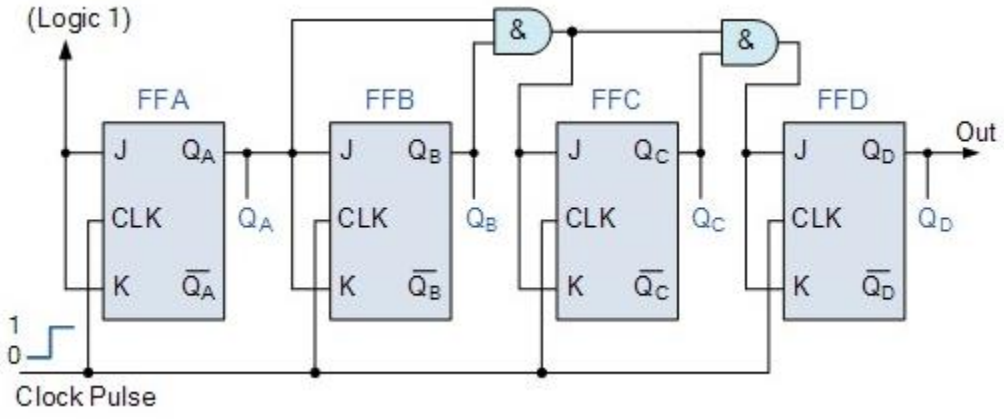
Answer:


Q5) Answer
0 1 1 0
CLK
Q0
Q1
Q2
Q3
Q4
0
1
0
1
1
Data bit will be stored after five pulses.
The procedure is kind a simple, data bit entered into the registers on first clock pulse and then shifted from left to right as the remaing bits entered and shifted the registers contains
Q4, Q3, Q2, Q1, Q0 = 11010
after five clockpulse.

Q6

Answer:

Logic Diagram for 4-stage Synchronous Binary Counter



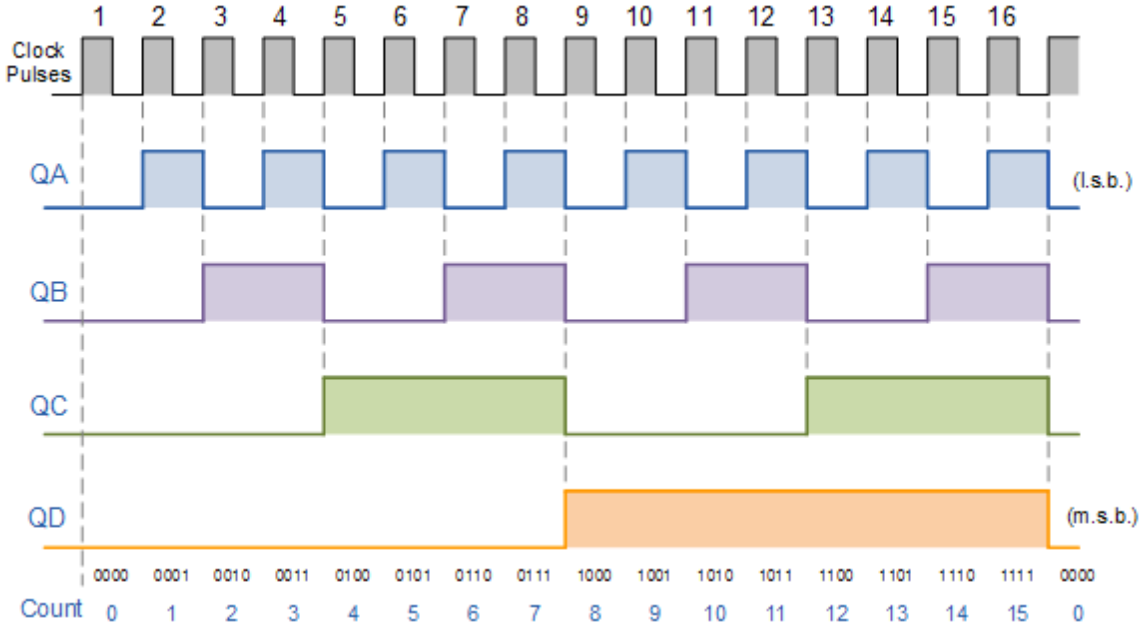
Explanation:

It can be seen above, that the external clock pulses (pulses to be counted) are fed directly to each of the J-K flip-flops in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.

The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.

As there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

Timing diagram for the 4-stage Synchronous Binary Counter



Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111). Therefore, this type of counter is also known as a 4-bit Synchronous Up Counter.

However, we can easily construct a 4-bit Synchronous Down Counter by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above. Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.