

Name - Saood ur Rehman

ID - 15031

Subject - Computer Architecture

Department - Bs (Cs)

Assignment No - 05

Question No. 01

Answer - There are various types of semiconductor memories. The most common is referred to as RAM (Random Access Memory). Most types have the property of RANDOM ACCESS MEMORY which means that it takes the same amount of time to access any memory location.

Here is a table of

semiconductor memory types

Memory type	Category	Erasure	write Mechanism	volatility
Random access memory RAM	Read write memory	Electrically byte level	Electrically	volatile
Read only memory (ROM)	Read only memory	Not possible	Marks	Non-Volatile
			Electrically	

2

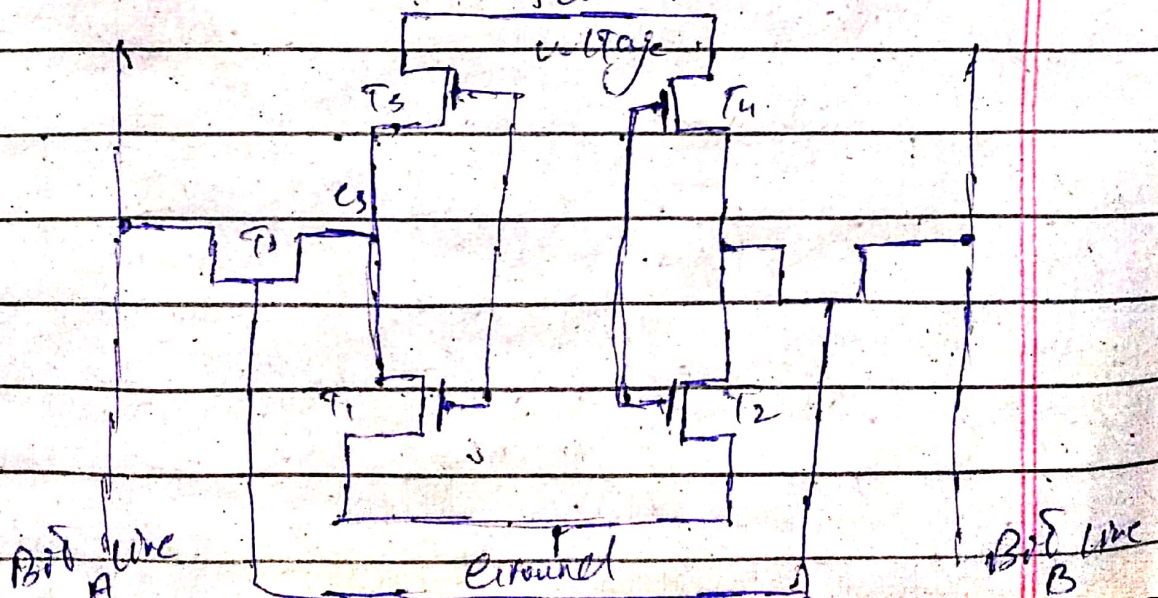
Programmable ROM (PROM)	Read	UV Light chip level		
Erasable PROM (EPROM)	Mostly memory	Electrically byte-level	Electrically	Non-Volatile
Electrically Erasable PROM (EEPROM)		Electrically block-level		
Flash Memory				

Answer (b)

Read Operation -

In SRAM for any operation to be performed, the word line should be high. To perform read operation initially, write operation -

Consider the memory bits consists of $Q = 0$ and $Q' = 1$



(3)

Answer (c)

Read Operation.

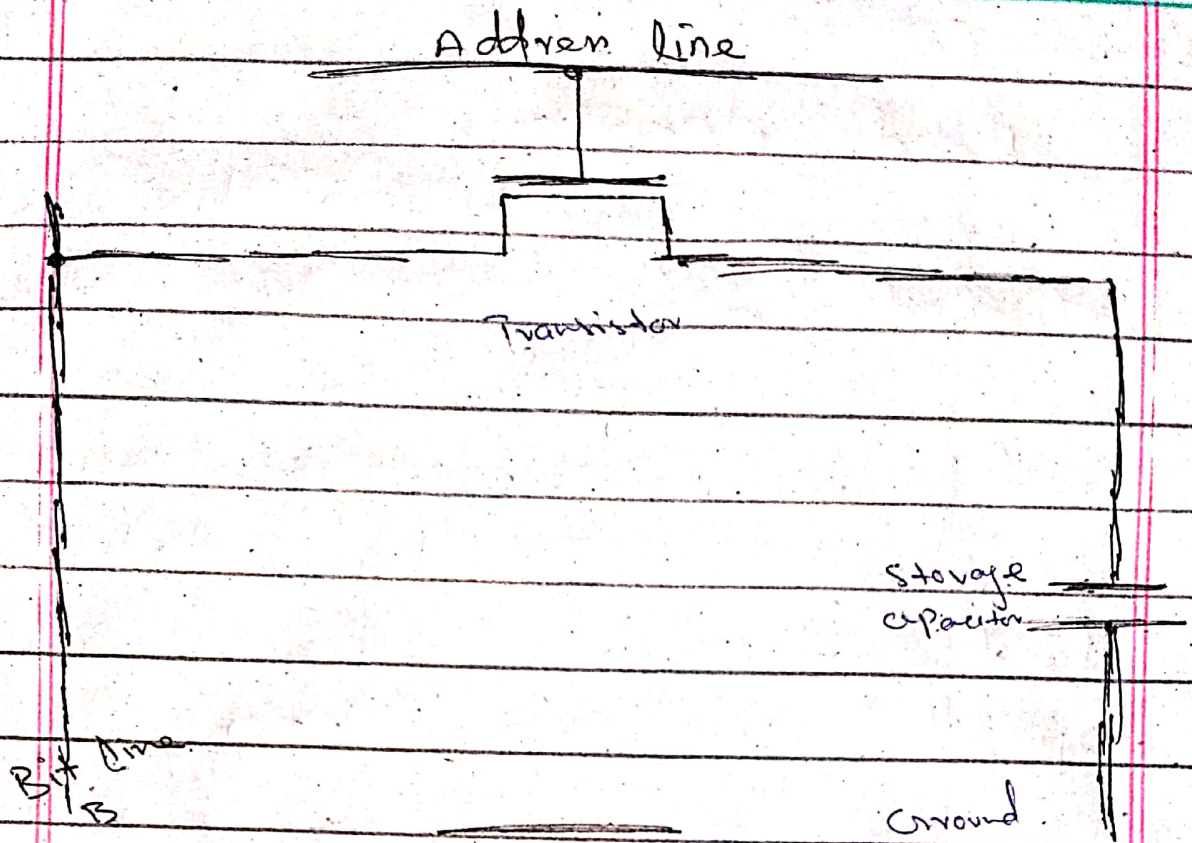
The address line is activated when the bit value from this cell is to be read or written. The transistor acts as a switch that is closed if a voltage is applied to the address line and open if no voltage is present on the address line.

write operation -

A voltage signal is applied to the bit line, a high voltage represents 1 and a low voltage represents 0. A signal is then applied to the address line allowing a charge to be transferred to the capacitor.

P.T.O

(4)



Answer No. (d)

16 - Mbit DRAM -

In this case 4 bits are reads or written at a time. Logically the memory array is organized as four square arrays of 2048 by 2048 elements. Various physical arrangements are possible. In any case, the elements of the array are connected by both horizontal and vertical lines. Each horizontal line connects to

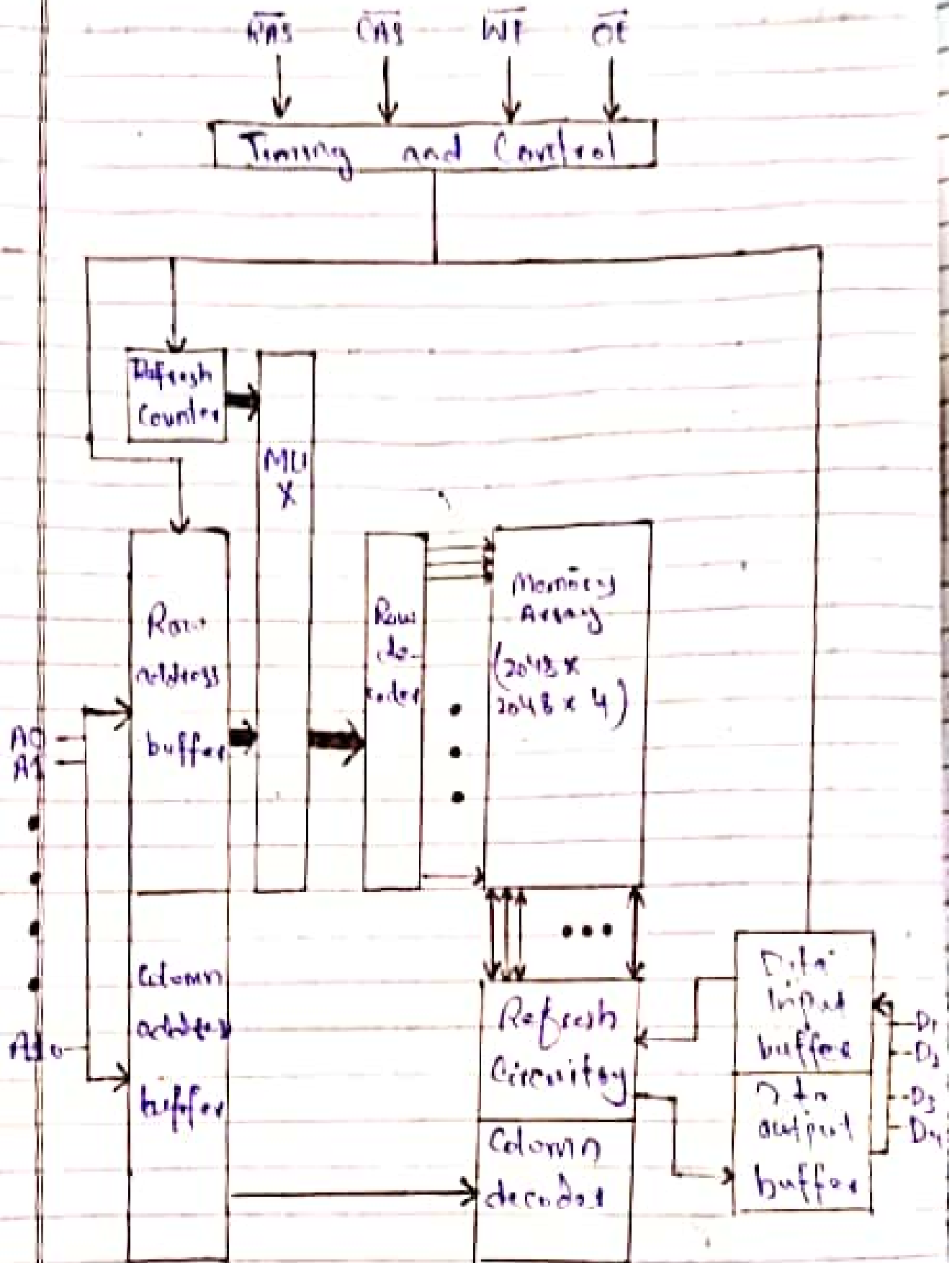
(5)

the select terminal of each vertical lines connects to the each cell in its row, each vertical lines connects to the Data - In/Source terminal of each cell in its column.

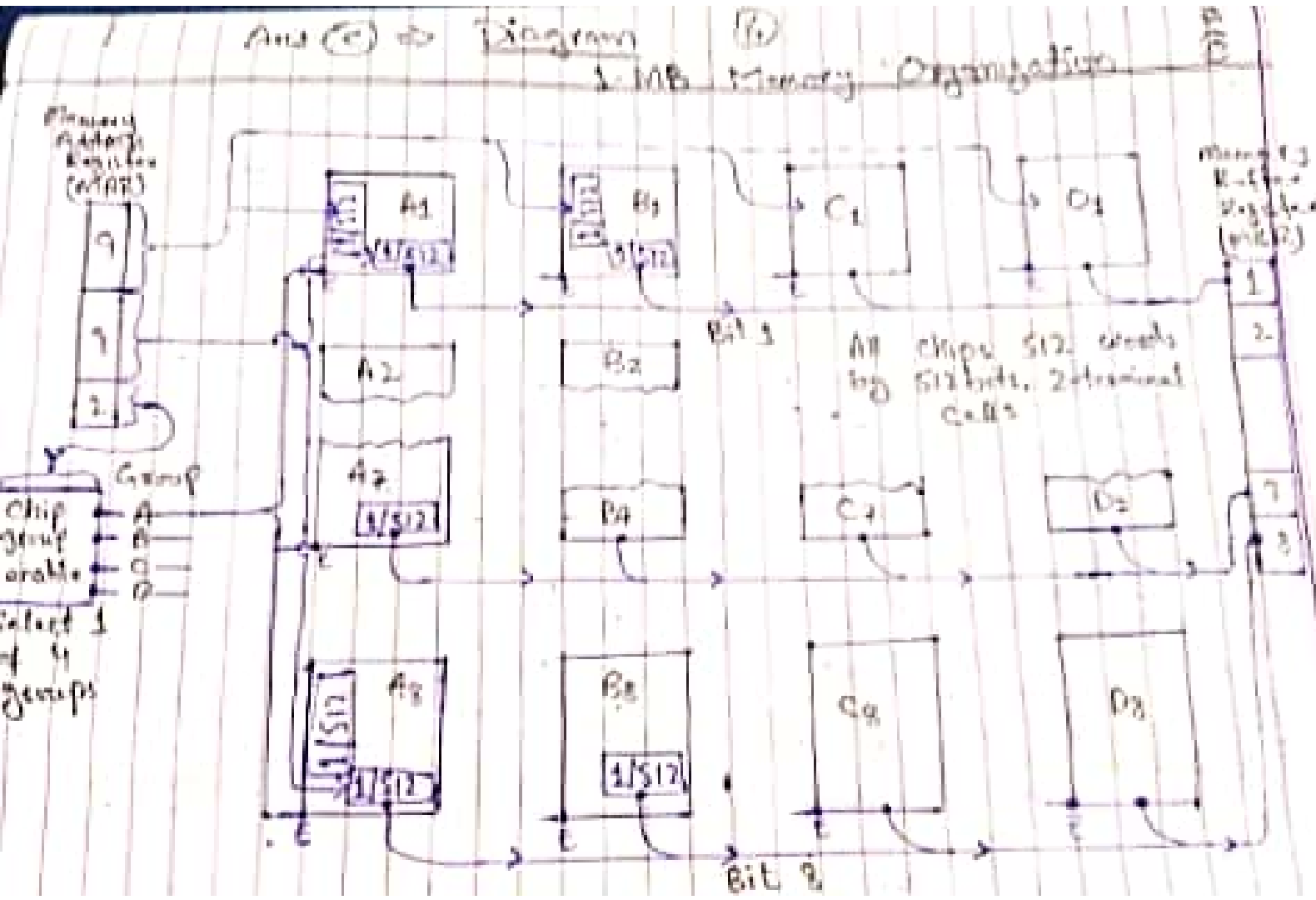
Because only 4bit are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

Diagram.

5



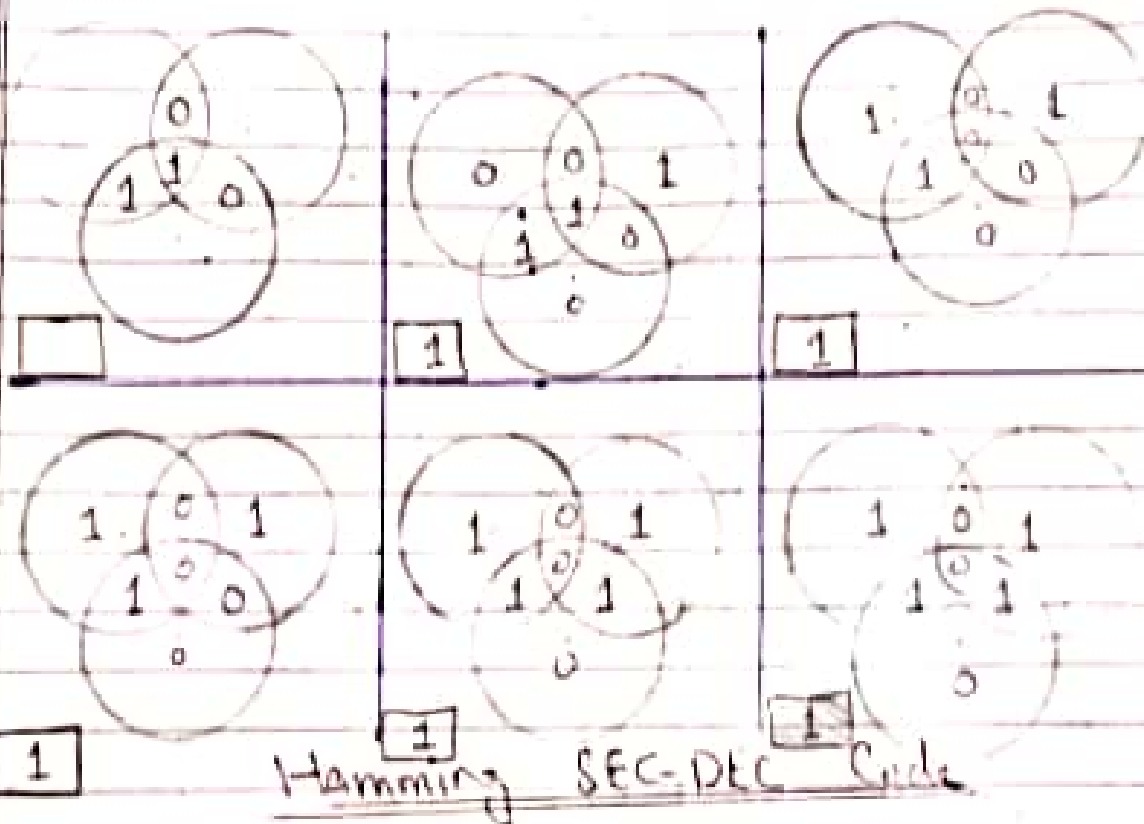
Ans (c) → Diagram (b) 1 MB Memory Organization



(7)

The possible organization of a memory consisting of $1M$ words by 8 bits per word. In this case can have four columns of chips, each column containing 256k words arranged.

Ans. (A)



With a 1-bit-per-chip organization, an SEC-DED code is generally considered adequate. For example, the IBM 30xx implementations used an 8-bit SEC-DED code for each 64 bits of data in main memory. Thus, the size of main memory is actually about 12% larger than is apparent to the user. The VAX computers

Used a 7-bit SEC-DED for each 32 bits of memory. for a 22% overhead. Contemporary DRAM system may have anywhere from 7% to 20% overhead.

Ans. (3)

Syndromes for the Hamming code interpreted as follows.

- (a) If the syndrome contains all 0s, no error has been detected.
- (b) If the syndrome contains one and only one bit set to 1, then an error has occurred in one of the 4 check bits. No correction is needed.
- (c) If the syndrome contains more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

Q2.

Ans. (a)

DRAM:

A dynamic RAM (DRAM) is made with cells that store data as charge on capacitors. The presence or absence of charge in a capacitor is interpreted as a binary 0 or 1. Because capacitors have a natural tendency to discharge, dynamic RAMs

(9)

require periodic charge refreshing to maintain data storage. The term dynamic refers to this tendency of the stored charge to leak away, even with power continuously applied.

SRAM:

A Static RAM (SRAM) is a digital device that uses the same logic elements used in the processor. In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations. A Static RAM will hold its data as long as power is supplied to it.

(b) EEPROM:-

Electrically erasable programmable read-only memory (EEPROM) is a read-mostly memory that can be written into at any time without erasing prior content only the byte or bytes addressed are updated. The write operation takes considerably longer than the read operation. EEPROM is more expensive than EPROM and also is less dense, supporting fewer bits per chip.

Flash memory:

Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. Flash memory does not provide byte level erasure.

Ans. (c) Hard Failure

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

Soft errors

A soft error is a random nondestructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles. Both hard and soft errors are clearly undesirable.