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Assignment

N#04

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(1)

(1) Answers each of the following.

A)

Ans:

Data processing:

Data can take a wide variety of forms and process requirement is broad.

Data storage:

Storing data a retrieving in memory.

Data movement:

Moving data from one to the other location i.e. main to secondary memory.

Control:

A control unit manages resources and orchestrates performance. Acting on instructions.

(2)

B)

Ans:

ISU:

Determine the sequence in which instructions are to be executed. (superscalar Architecture)

IDU:

Fetch from IFU buffer and is responsible for the parsing and decoding all instructions and operation code.

LSU:

Responsible for handling all types of operand accesses of length.

XU:

Translate logical address from instruction into physical address in main memory.

FXU:

Executes fixed point arithmetic operations.

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B.FU:

Handle all binary  
Hexadecimal floating

D.FU:

Handle Fixed and  
float points

RU:

Keep copy of the  
complete state of system  
that include all registers.

COP:

Responsible for data  
compression and encryption.

L-Cache:

64 Kb L1 Instruction  
Cache allow IPU to fetch  
Instruction.

L2 control:

Control logic  
that manage traffic

L2 Data:

1 MB L2 data  
Cache for all memory

(U)

traffic other than instructions.

Inst. L2:

L1 L2  
Instruction cache.

C)

Ans:

IAS operates by performing instruction cycle each consist of two sub-cycles.

opcode of next instr is decoded in IR

and address portion is decoded in MAR. This

instruction maybe taken from ISR,

The control circuitry interpret opcode and execute the instruction, by ALU.

D)

Ans:

⇒ (A)

No. these programs

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are never considered to be embedded because they are not integral component.

⇒ (b): yes, the software within the disk drive control HDA hardware and is hard real time as well.

⇒ (c): NO, I/O drivers do not represent embedded system

⇒ (d): yes, PID A is embedded system

⇒ (e): yes, the firmware in cell phone is controlling the radio hardware.

⇒ (f): yes, these computers were the most powerful and very large. The software running in these computers control the accelerator hardware.

⇒ (g) FMS is not embedded if FMS is not connected to avionics and is used only for logistic computerization.

⇒ (h) yes, both are embedded

⇒ (i) yes, in this case system is embedded

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⇒ (J) Engine is part of a large system and directly controlled through hardware so "yes".

Q: No: 02:

Ans:

⇒ (A) There are four main structures.

i CPU: Central processing unit control operation of computer

ii Main Memory: Store memory

iii I/O: Move data between computer and external environment.

iv System Interconnection: provide communication between CPU and I/O.

⇒ (B) The characteristics are as follows.

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⇒ Identical instruction set:  
Lower family has set  
that is subset of  
Higher family so programs  
can move up but not  
down.

⇒ Identical operating system:  
Some OS are similar  
for all family members.

⇒ Increasing speed: Increases  
as we go from lower  
to higher family.

⇒ Number of I/O ports:  
Increases from lower to  
higher family members.

⇒ Memory size: Increases  
from lower to higher  
family members.

⇒ Cost: Increase from  
lower to higher  
family members.



(C) Stored - program - Concept was first implemented in "IAS" by John van Neuman. First publication of idea was in 1945 for a new computer (EDVAC)

- It consist of:
- 1 Main Memory:
  - 2 Arithmetic Logic Unit:

(D) This De Moo's Law was given by cofounder of intel Gordon Moore in 1965. He observed that number of transister are doubling on chip every year.

Consequences:

- 1: Cost has fallen at dramatic rate
- 2: The speed has been increasing.
- 3: Computers are becoming smaller
- 4: Reduction in power
- 5: Fewer inter chip connections.

Q: NO: 03:

A:

=> Computer Architecture:  
 Refers to attributes that are visible to programmers

=> Attributes that have direct impact on logical execution

Computer Organization:

=> Refers to operational units and their inter-connection.

=> I/O mechanism, instruction set etc.

B:

CISC:

- (1) Large Instruction set
- (2) Complex processor, requiring millions of transistors.
- (3) Intel, AMD,

RISC:

- (1) Simple single cycle
- (2) Few instruction and transistors are required. Thus cost is low
- (3) Apple Mac G3, Power PC.

C:

Micro processor.

- (1) Heart of computer system
- (2) Only a processor. Other components have to be connected.

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- (3) Cannot be used in Compact System
- (4) Cost increases.

### Micro Controller:

- (1) Heart of embedded system
- (2) Has external processor along with memory and I/O
- (3) The circuit is small
- (4) Cost is low.

D:

### Cortex A:

- ⇒ Cortex A is a application processor
- ⇒ Used in smart phones mostly. Also digital TV etc

### Cortex R:

- ⇒ Cortex R is design

(2)

for real time applications.

=> It has a high clock frequency and low latency time.

Cortex M:

=> Cortex M is developed for microcontrollers.

=> Designed for lowest gate count and lowest possible power consumption.

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Q: NO: 04:

A: Part A

Content are divided  
into 5 bit of two  
Instructions,

LH, RH

LH = 010FA

OP code = 01

address = 0FA

(14)

RH = 210FB  
opcode = 21  
address = 0FB

Now converting to  
binary

LH:

01 = 00000001 = Load(M)  
M(0) = 0FA

First 5 bit of 08A  
should read Load M(0FA)

RH:

24 = 00100001 = Store M(x)

M(x) = 0FB

Second 5 bit should  
read on STORE M(0FB)

Assembly code for  
08A is:

(010FA210FB)

Load M(0FA)

STORE M(0FB)

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(2)

LH = 010FA  
opcode = 01  
Address = 0FA

RH = 0F08D  
opcode = 0F  
Address = 08D

Converting:

LH:

01 = 00000001 =  
Jump + M(x, 0:19)  
Address location 08D

Second 5 bit should  
Read on Jump + M(08D,  
0:19)

Assembly code for 08B =

010FA0F08D  
Load M(0FA)  
Jump + M(08D; 0:19)



(3)

LH = 020FA

Op code = 02

Address = 0FA

RH = 210FB

Op code = 21

Address = 0FB

LH:

02 = 0000010 = Load-M(x)

Refer to 0FA

First 5 bit should read for 08c

Load - M(0FA)

RH:

21 = 00100001 = STOR M(x)

M(x) = 0FB

Second 5 bit should read of 08c  
STOR(0FB)

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Assembly code = 020FA210FB

Load = M(0FA)

STOR - M(0FB)

Part:

B:

(1) In 08A address  
The M(0FA) transfer  
transfer to accumulator  
and transfer content  
to 0FB

(2) In 08B address  
The M(0FA) transfer  
to accumulator and  
take next instruction  
from left half of  
M(08B)

(3) In 08C address  
The M(0FA)  
transfer to accumulator  
and transfer content  
to memory location  
0FB