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Subject : Computer Architecture

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(Q No 1)

Ans "A"

Different desktop applications that require the great power of Contempory microprocessor based System are:

- ✔ Image Processing
- ✔ Three-dimensional rendering
- ✔ Speech recognition
- ✔ Video Conferencing
- ✔ Multimedia authoring
- ✔ Voice and video annotation of files
- ✔ Simulation modelling

"B"

Ans: The Techniques used in contemporary processor to we increase Speed are following.

* **pipelining:** pipelling enables a processor to increase Speed Simultaneouly on multiple instruction by perporming of different pase at the Same time.

* **Branch prediction:**

Branch prediction potentially increases the amount work of available for the processor to execute.

* **Data flow analysis:**

The processor analysis with instruction are dependent on eache others results or data to create or Shedules of instructions.

* **Specualative execution:-**

This enables the processor to keep its execution engines as busy as possible by that are likely to be needed.

"C"

Ans Dissuss the problems created due to increase in clock speed and logic density of the processor are

- **Power:** As the density of logic and the clock speed on a chip increase so the power and also dessipated the heat.
- **RC delay:** The speed at which electrons can flow on a chip between transister is limited by the resistance and capacitance of the metal wire connecting them. as the RC are product increases.
- **Memory latency:**

Memory Access Speed (latency) and transfer Speed throughout) lags processor Speeds

"D"

Ans: The Speedup using a parallel processor with N processors that fully exploits the parallel portion of the program is as follows:

Speedup = Time to execute program on a single processor / Time to execute program on /N parallel processors

$= T(1-f) + Tf / T(1-f) + Tf/N = 1/(1-f) + f/N$

(3)

"E"

Ans: Multicore:-

- The use of multicore multi processor on the same chip provides the potential to increase performance without increasing the clock rate.
- With two processors larger caches are justified.
- As caches became larger it made performance sence to create two and then three levels of cache on a chip

Mic:

- Leap in performance as well as the challenges in developing software to exploit such a large number of ~~cost~~ cores.
- The multicore and MIC Strategy involves a homogenous collection of general purpose a single chip.

Gpu:

- Core designed to perform parallel operation on graphics data.
- Used as vector processor for a variety of Application that require repetitive computations.

(Q No 2)

Ans: Effective CPI:

$CPI = (1*46000) + (2*33000) + (2*16000) + (1*90000)/100$

$CPI = 162000/100$ $CPI = 1620$

Mips Rate:

Mips Rate = $60\ MHz / 1620 * 10^6$

④

Mips rate = $60 * 10_6 / 1620 * 10_6$

Mips rate = $60 / 1620$

Mips rate = 0.037

Execution Time:

$T = Ic / (Mips * 10_6)$

$T = 104000 / (0.037 * 10_6)$

$T = 104000 / 37 * 10_3$

$T = 2811 * 10_3$

$T = 2.811$ Sec

Ans:- "B"

For machine A:

$CPI = (1*8 + 3*4 + 2 + 3*4) * 10_6 / (8+4+2+4) * 10_6$

$CPI = 40 * 10_6 / 18 * 10_6$

CPI = 2.22

Mips rate = 200 MHz / $2.22 * 10_6$

Mips rate = $200 * 10_6 / 2.22 * 10_6$

Mips rate = 90

$T = Ic / (Mips * 10_6)$

$T = 18 * 10_6 / 90 * 10_6$

$T = 0.2$ Sec

For Machine B:

$CPI = (1*10 + 2*8 + 4*2 + 3*4) * 10_6 / (10+8+2+4) * 10_6$

$CPI = 46/24$

$CPI = 1.92$

(5)

Mips rate = 104

$T = Ic / (Mips * 10^6)$

$T = 24 * 10^6 / 104 * 10^6$

$T = 0.23$ sec

Ans "C"

The Mips rate could be computed as the following:

Mips rate = $Ic/T * 10^6$

$Ic = Mips\ rate * T * 10^6$

Now by computing the ratio of the instruction count of the IBM RS/6000 to the VAX 11/780 which is:

$18 * 1x * 10^6 / 1 * 12x * 10^6$

$= 18/12$

$= \underline{1.5}$

Ans "b"

Regarding to the VAX 11/780 the CPI:

$CPI = (5\ MHz) / (1 * 10^6) = 5 * 10^6 / 1 * 10^6$

$= 5/1 = \underline{5}$

Regarding to the IBM RS/6000 the

$CPI = (25\ MHz) / (18 * 19) = 25 * 10^6 / 18 * 10^6$

$= 25/18 = \underline{1.4}$

(5) "1"

Ans) a Since have the same instruction rate that mean the additional instructions for each task between the instruction types Base for the following tables gotten.

Instruction Type	CPI	instruction Mix
Arithmetic and logic	1	60%
Load/store with Cache hit	2	18%
Branch	4	12%
Memory reference with Cache miss	12	10%

The average CPI = (1x0.6) + (2*0.18) + (4x0.12) + (12x0.1) = 2.64

Where fore has the CPI has been increased since the time for memory access as also increased

(b) Mips = 400/2.26 = 152 there is a Corresponding drop in the Mips rate.

(c) The Speedup factor equals to the ratio of the Execution times the execution time is calculated as the following $T = Ic/(Mips * 10^6)$

for the one processor $T_1 = (2 * 10^6)/(178 * 10^6) = 11$ ms

for the 8 processor executed 1/8 of the million instruction plus the 25,000

$T_8 = 2 * 10^6 \div 8 + 0.025 * 10^6/152 * 10^6$

$T_8 = 1.8$ ms

Therefore we have

Speedup = Time to execute program on a single processor / Time to execute program on N parallel processor

Speedup = 11/1.8

Speedup = 6.11

(d.) By depending on the information given it is not obvious how to quantify his effect in Amdahl's equation. Therefore if it is supposed that the fraction of code which is parallelizable is f = 1 then Amdahl's law decreases to Speedup = N = 8 Therefore the actual Speedup is only about 75% of the theoretical Speedup

[The End]