Name Muhammad Saqib Khalil

ID 13342

Subject DLD

program BE Electrical

Exam Summer (2020) Final

Date 24/09/2020

Submitted to: Engr. Dr. Jehenzeb Khan.

Q#1 (a)

$$F(A,B,C,D) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$$

	A	B	C	D		
0	0	0	0	0	1	$\bar{A}\bar{B}\bar{C}\bar{D}$
1	0	0	0	1	1	$\bar{A}\bar{B}\bar{C}D$
2	0	0	1	0	1	$\bar{A}\bar{B}C\bar{D}$
3	0	0	1	1	0	$\bar{A}\bar{B}CD$
4	0	1	0	0	1	$\bar{A}B\bar{C}\bar{D}$
5	0	1	0	1	1	$\bar{A}B\bar{C}D$
6	0	1	1	0	1	$\bar{A}BC\bar{D}$
7	0	1	1	1	0	$\bar{A}BCD$
8	1	0	0	0	1	$A\bar{B}\bar{C}\bar{D}$
9	1	0	0	1	1	$A\bar{B}\bar{C}D$
10	1	0	1	0	0	$A\bar{B}C\bar{D}$
11	1	0	1	1	0	$A\bar{B}CD$
12	1	1	0	0	1	$AB\bar{C}\bar{D}$
13	1	1	0	1	1	$AB\bar{C}D$
14	1	1	1	0	1	$ABC\bar{D}$
15	1	1	1	1	0	$ABCD$

Q 6

$$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D}$$
$$+ A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D}$$

$$= \bar{A}\bar{B}\bar{C}(\bar{D}+D) + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}(\bar{D}+D) + \bar{A}BC\bar{D} +$$
$$A\bar{B}\bar{C}(\bar{D}+D) + AB\bar{C}(\bar{D}+D) + ABC\bar{D}$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}CB(\bar{B}+B) + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C} +$$
$$ABC\bar{D}$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}C\bar{D} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC\bar{D}$$

$$\Rightarrow \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}C\bar{D} + A\bar{B}\bar{C} + AB\bar{C} + ABC\bar{D}$$

$$\Rightarrow \bar{A}\bar{C}(\bar{B}+B) + \bar{A}C\bar{D} + A\bar{C}(\bar{B}+B) + ABC\bar{D}$$

$$= \bar{A}\bar{C} + \bar{A}C\bar{D} + A\bar{C} + ABC\bar{D}$$

$$= \bar{A}\bar{C} + A\bar{C} + \bar{A}C\bar{D} + ABC\bar{D}$$

$$= \bar{C}(\bar{A}+A) + \bar{A}C\bar{D} + ABC\bar{D}$$

$$= \bar{C} + \bar{A}C\bar{D} + ABC\bar{D}$$

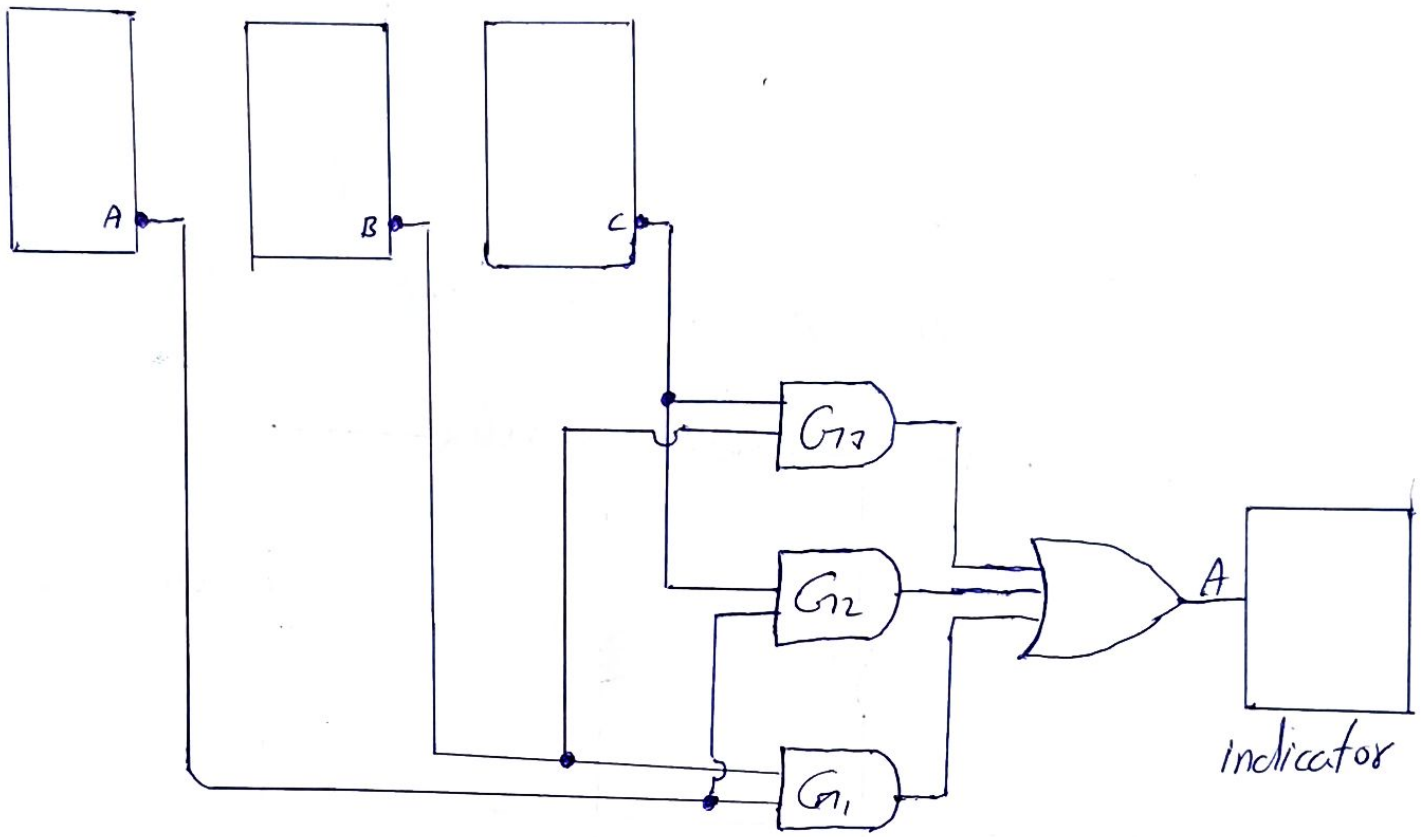
$$= \bar{C} + C\bar{D}(\bar{A}+AB)$$

$$= \bar{C} + C\bar{D}(A+B)$$

Q#1

(b)

Sol:-



Theory of logic circuit:

The AND-OR circuit in above fig has inputs from the sensors on tank A, B & C as shown. The AND gate G_1 checks the level in

in tonks A & B, gate G_2 checks tanks A & C, & gate G_3 checks tanks B & C. When chemical level in any two of the tanks gets too low, one of the AND Gates will have Highs on both of its inputs causing its output to be HIGHs and so the final output X from the OR gate is HIGH This HIGH input is then used to activate an indicator such as lamp or alarm.

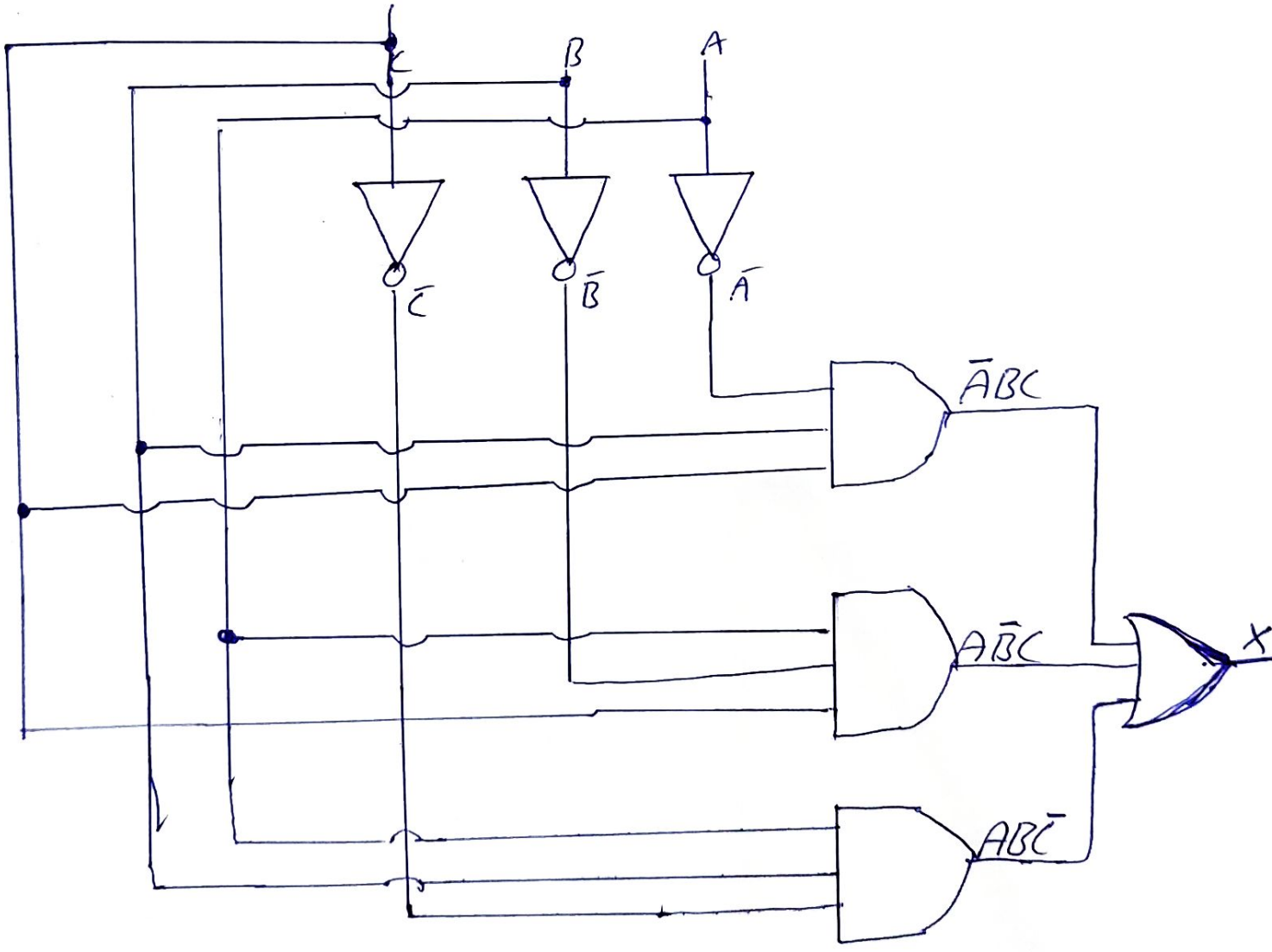
Q#2 (a)

Sol:

Notice that $X=1$ for only of the two input condition. Therefore the logic expression is

$$X = \bar{A}BC + A\bar{B}C + AB\bar{C}$$

The logic gates required are three invertor three input AND Gates & one 3 input OR Gate.



Q#2
(b)

Solution:-

The expression for the output of the circuit is

$$X = \overline{\overline{(ABC)}}C + \overline{\overline{A}}\,\overline{\overline{B}}\,\overline{\overline{C}} + D$$

Applying deMorgen's theorm & Boolean algebra,

$$X = (\bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}})C + \bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}} + D$$

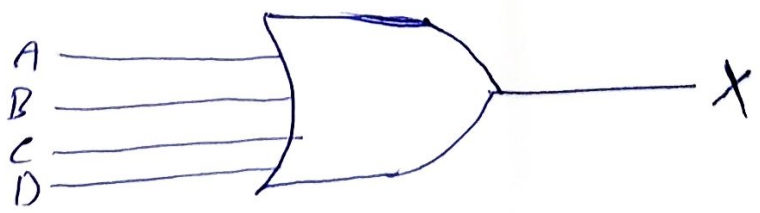
$$= AC + BC + CC + A + B + C + D$$

$$= AC + BC + C + A + B + C + D$$

$$= C(A + B + 1) + A + B + D$$

$$\boxed{X = A + B + C + D}$$

The simplified circuit is a 4-input OR gate is:-



Q#3

a)

Sol:-

out of sixteen possible combinition of four variables, the combination in which there are exactly three 1s are listed in Truth table with corresponding product term for each.

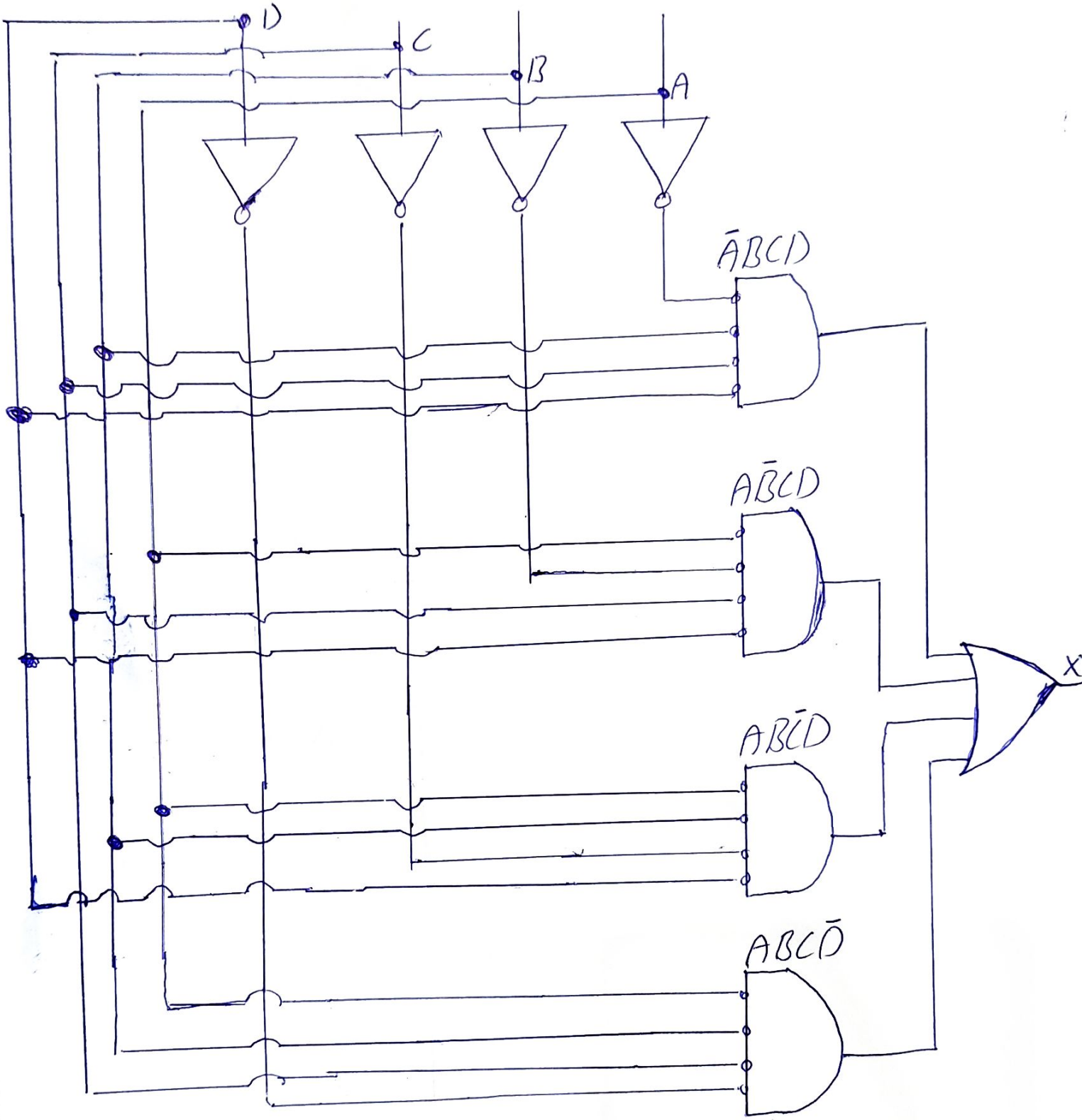
T. Table.

A	B	C	D	product term
0	1	1	1	$\bar{A}BC1$
1	0	1	1	$A\bar{B}C1$
1	1	0	1	$AB\bar{C}1$
1	1	1	0	$ABC\bar{D}$

The product terms are ORed to get the following expression

$$X = \bar{A}BC1 + A\bar{B}C1 + AB\bar{C}1 + ABC\bar{D}$$

This expression is implemented with AND OR Logic



Q#3 (b)

Decoder:

Decoder is combinational logic circuit that convert the binary integer to the associated pattern of output bits. it has n inputs & 2^n outputs.

OR

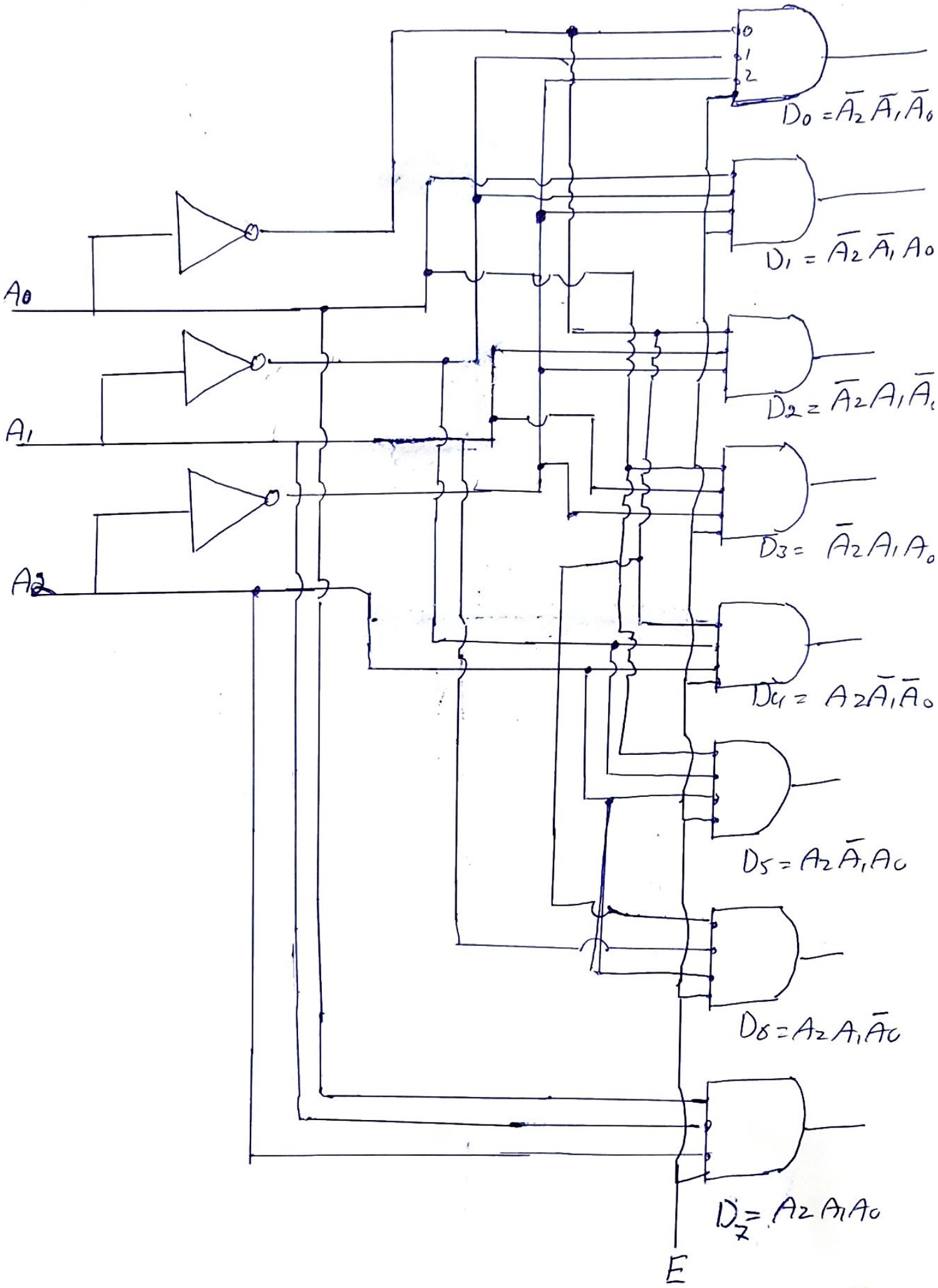
Decoder accepts values and decode it

* output corresponds to value of n inputs

Decoder consist of

1) input (n)
2) output (2^n, numbered $0 - 2^n - 1$)
3) selector / Enable (achive high or achive low)

3 to 8 line decoder with enable:-



Q#4

a)

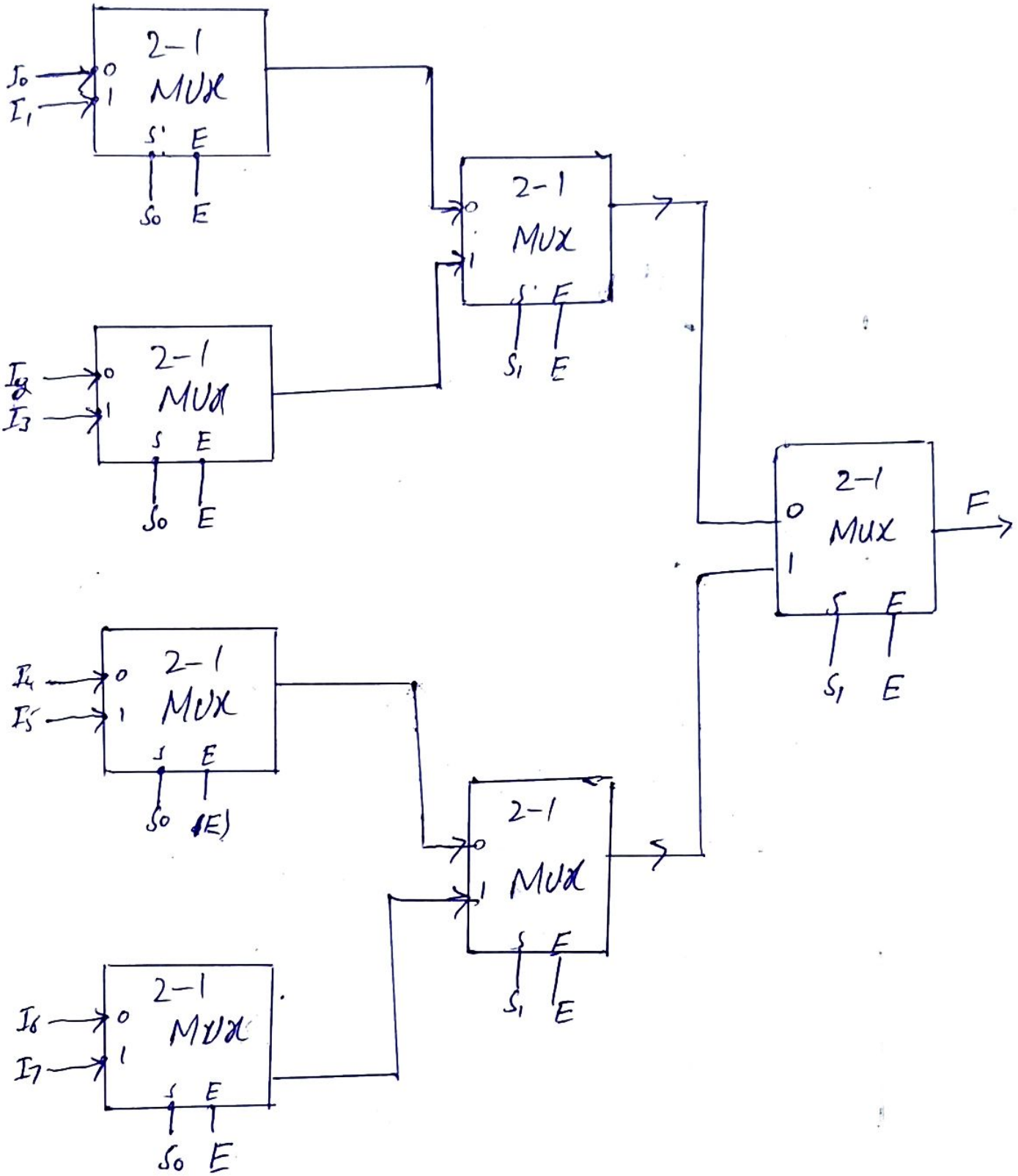
Multiplexer (MUX):-

A Multiplexer can use addressing bits to select one of several input bits to be output.

* A selector chose a single data input & passes it to the MUX output
* It has one output at a time
* MUX uses n binary select bits to chose from a maximum of 2^n unique input lines.
* The output of mux is the data input whose index is specified by the n bit code
* Multiplexer consist of:

① inputs (multiple) $= 2^n$
② output (Single)
③ Selector (No. depends on No. of input) $= n$
④ Enable (active high or active low)

8 to 1 MUX using 2 to 1 MUX:-



Q#4

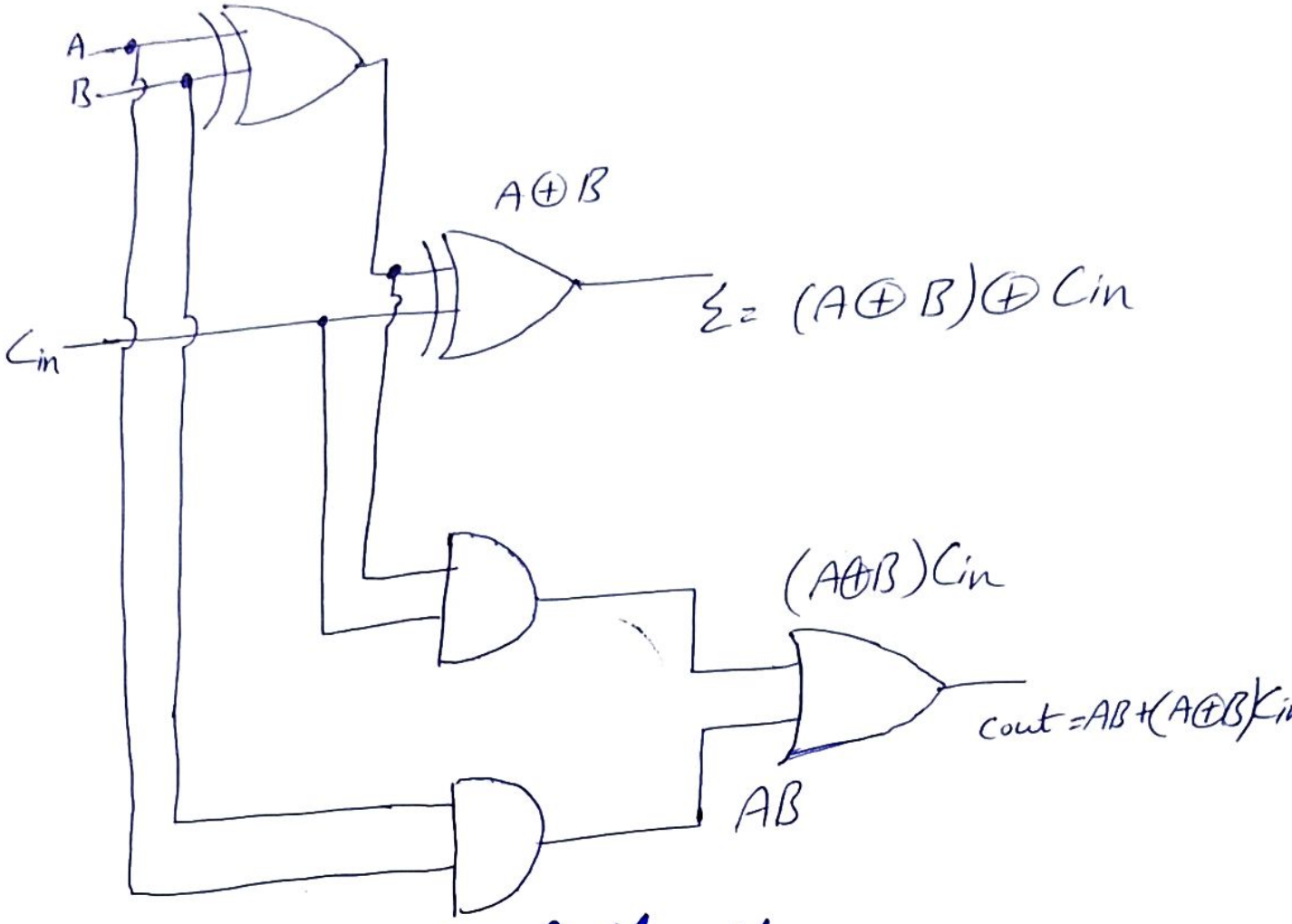
(b)

Difference between Half adder & full Adder:-

The major difference between Half adder & full Adder is that Half Adder adds two 1-bit numbers given as input but do not add the carry obtained from previous addition while the full adder along with two 1-bit numbers can also add the carry obtained from previous addition.

Half adder & full adder both are combinitional logic circuit but differs in the way they process the inputs. A combinitonal circuit is one which does not consist of any memory elements

Logic circuit:-



Truth Table of Full Adder

A	B	Cin	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Expression of full Adder:-

$$\text{Sum} = C(\overline{A \oplus B}) \oplus \bar{C}(A \oplus B)$$

$$\text{carry} = C(A \oplus B) + AB$$

Q.5 (a)

Difference between Combinational & Sequential circuit

Combinational Circuits	Sequential Circuits
① The output depends only upon the present input and there is no need for feedback for input & output so memory element is not required	The output depend upon both present input & present state (previous output), so memory element is required to save the feedback state
② It is easier to design, use & handle.	It is not easier to design use & handle than combinational circuits.
③ Clock signal are not required and it is not dependent on time	Clock signal are required & it is dependent on time & clock so need triggering
④ Elementary building blocks are only Logic gates.	Elementary building blocks are Flip-Flops
⑤ These are faster Logic circuit	These circuits are slower than combinational circuit.

Combinational circuit Example.

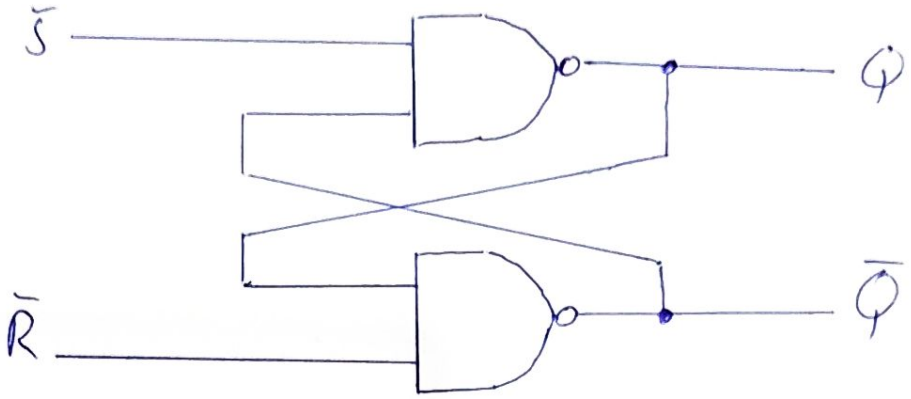
1. Half Adder
2. Full Adder
3. multiplexer
4. Decoder

Sequential Circuit Example.

1. Flip Flop
2. Register
3. Counter
4. Clocks.

Q#5 (b)

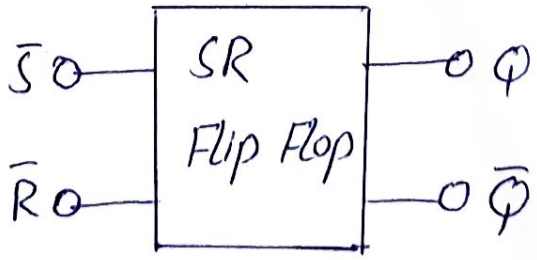
RS Latch using NAND Gate Logic diagram:-



Function Table:

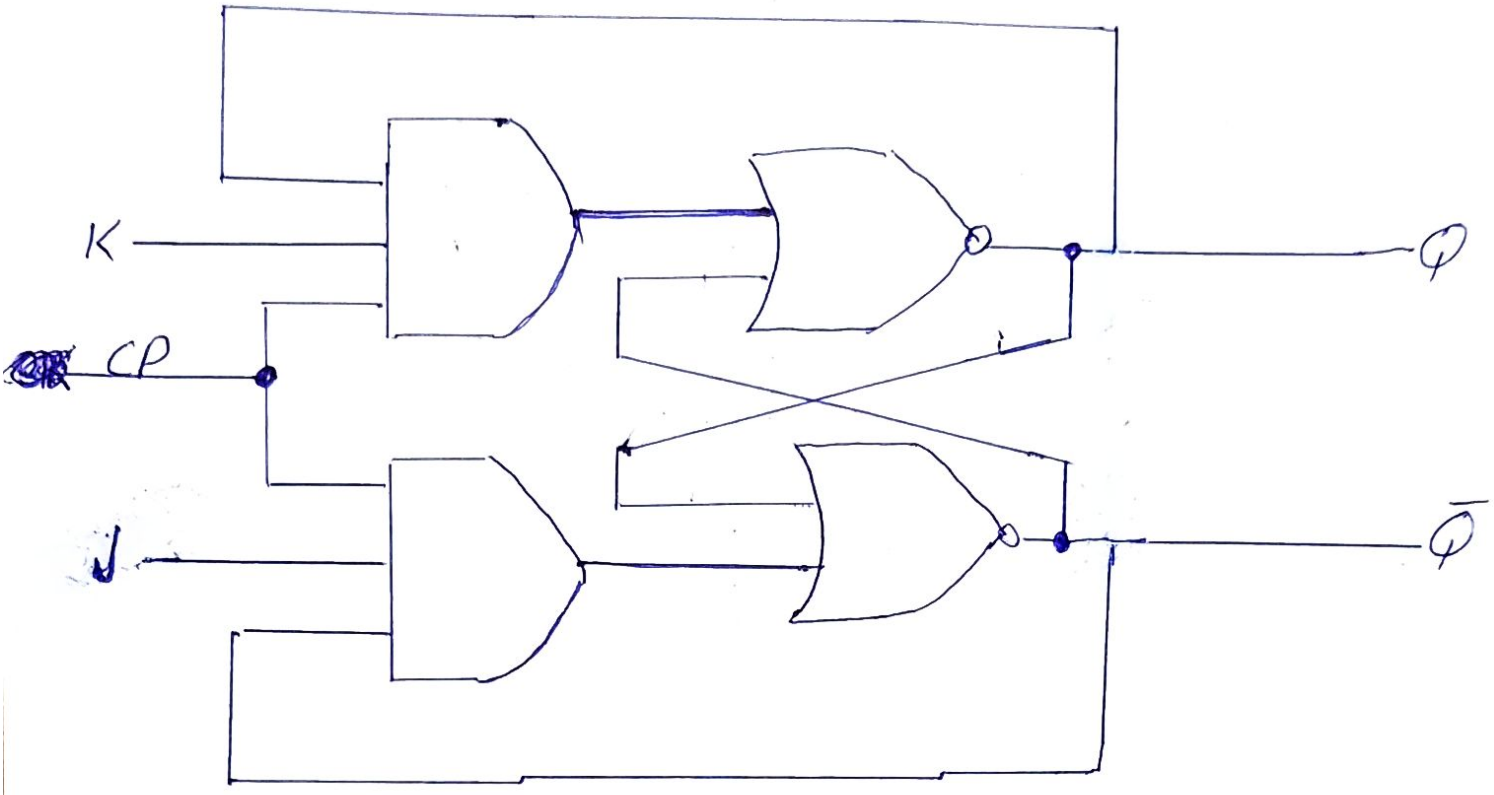
Inputs		Outputs		Comments
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
1	1	NC	NC	No change, latch remain at present state
0	1	1	0	Latch set
1	0	0	1	Latch Reset
0	0	1	1	invalid condition

Symbol:-



Q(5)(c)

JK Flip Flop logic Circuit:-



Characteristic Equation of JK Flip Flop:-

$$Q(next) = J\bar{Q} + \bar{K}Q$$

OR

$$Q(t+1) = \bar{K}(t)Q(t) + J(t)\bar{Q}(t)$$