Name = M. Usama

ID = 14150

Subject = VLSI Technology

Submitted To = Engr: Zulqarnain.

Semesster = 6th

Date = 25/6/20

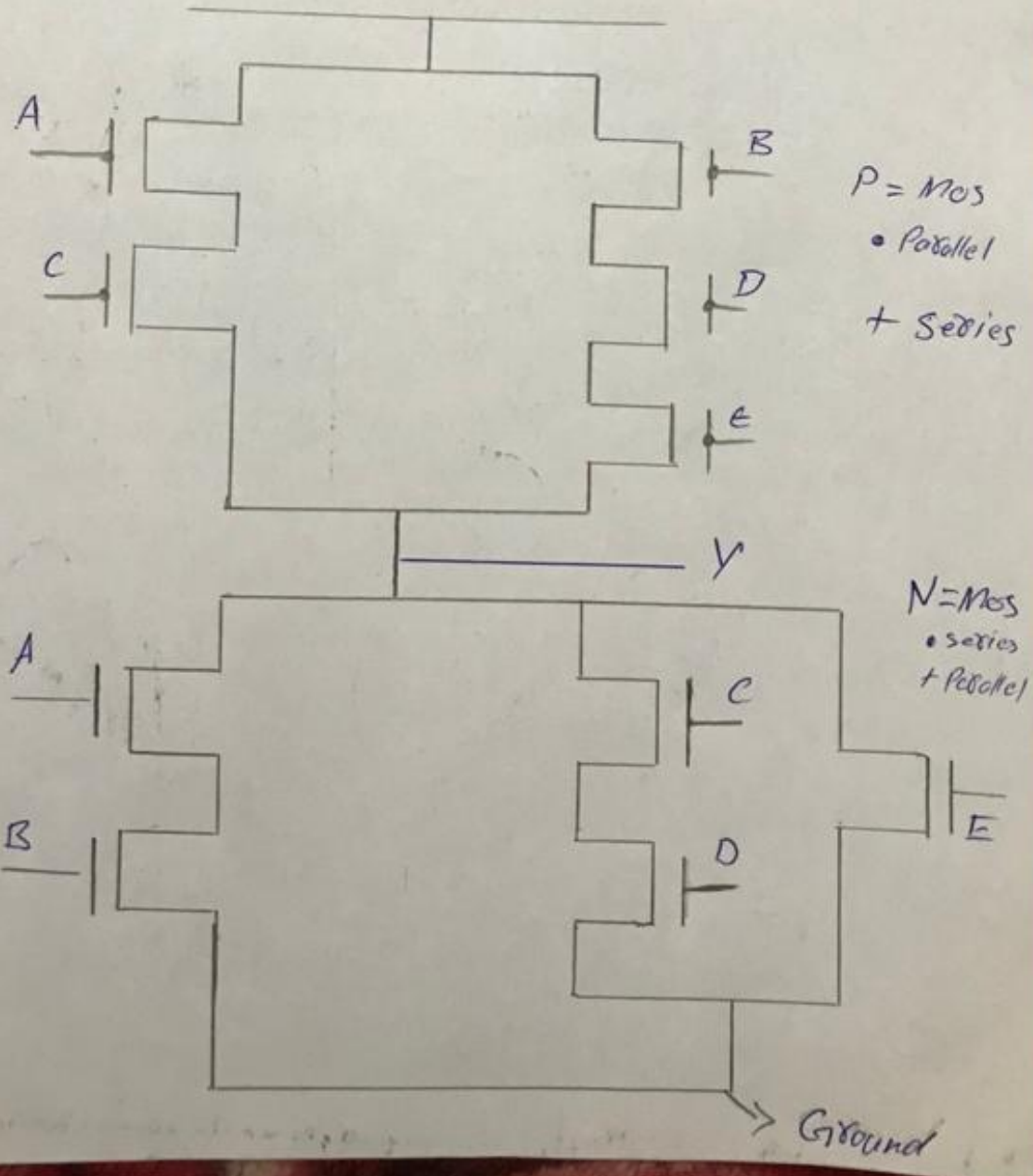
Q = 1 Design an area effcient Layout for CMOS shown below

$$F = AB + (C+D)E$$

N = • Series
N = + Parallel

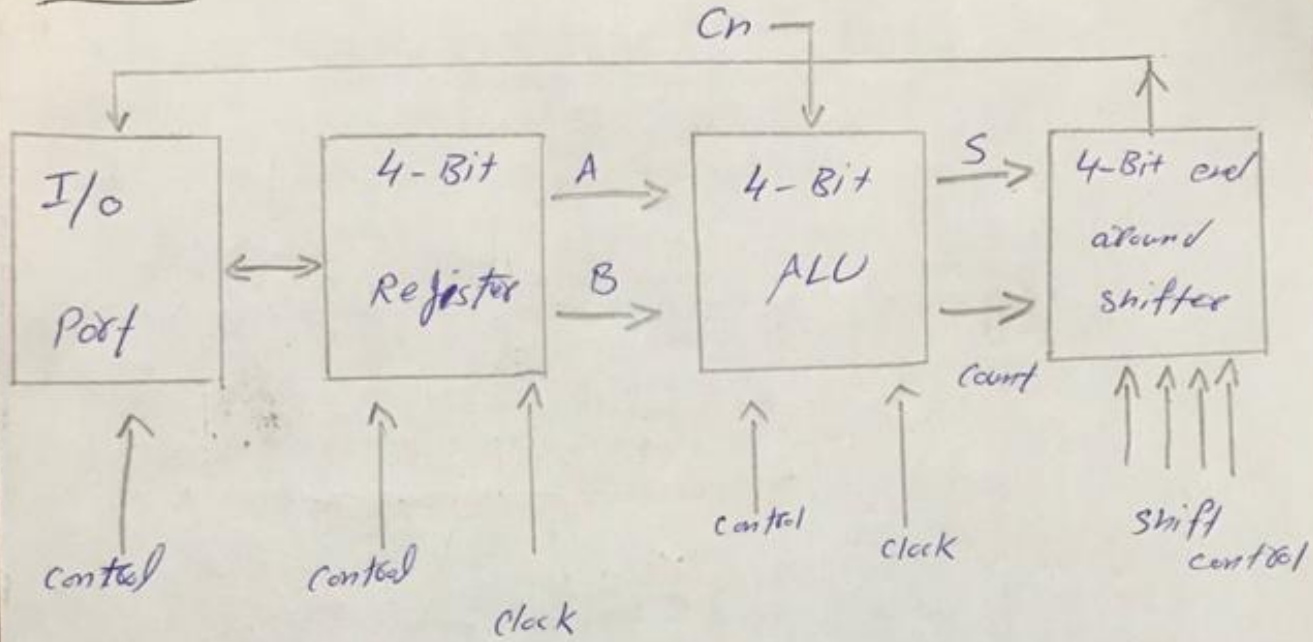
P = • Parallel
P = + Series

$F = AB + (C \cdot D)E$



M-Usama 2 14150

Q = 2



design Subsystem design consideration. of 4-Bit order.

P- T.O

Design of 4-Bit adder.

Inputs			outputs	
Ak	Bk	Ck-1	Sk	Ck
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Q = 3

(A) VLSI Design Issues & Design trends.

Ans Some Architectural Issues in VLSI Design :-

In all design Process, a logical & systematic approch is essential. This is particularly so the case of the design of a VLSI system which could otherwise take so long as to rendered the whole system absolete before it is off the drawing board.

But now some sensible concepts applied in a larger system design requirements.

Guideline set as follows

(1) Define the requirment (Properly & carefully)

(2) Partition the overall architecture into appropriate subsystem.

(3) consider communication paths carefully in

order to develop sensible interelationship b/w subsystem.

(4) Draw a floor plan of how the system is to map into the silicon (and alternate between 2, 3 & 4 as necessary).

(5) Aim for regular structures so that Design is largely a matter of replication.

Q = 3

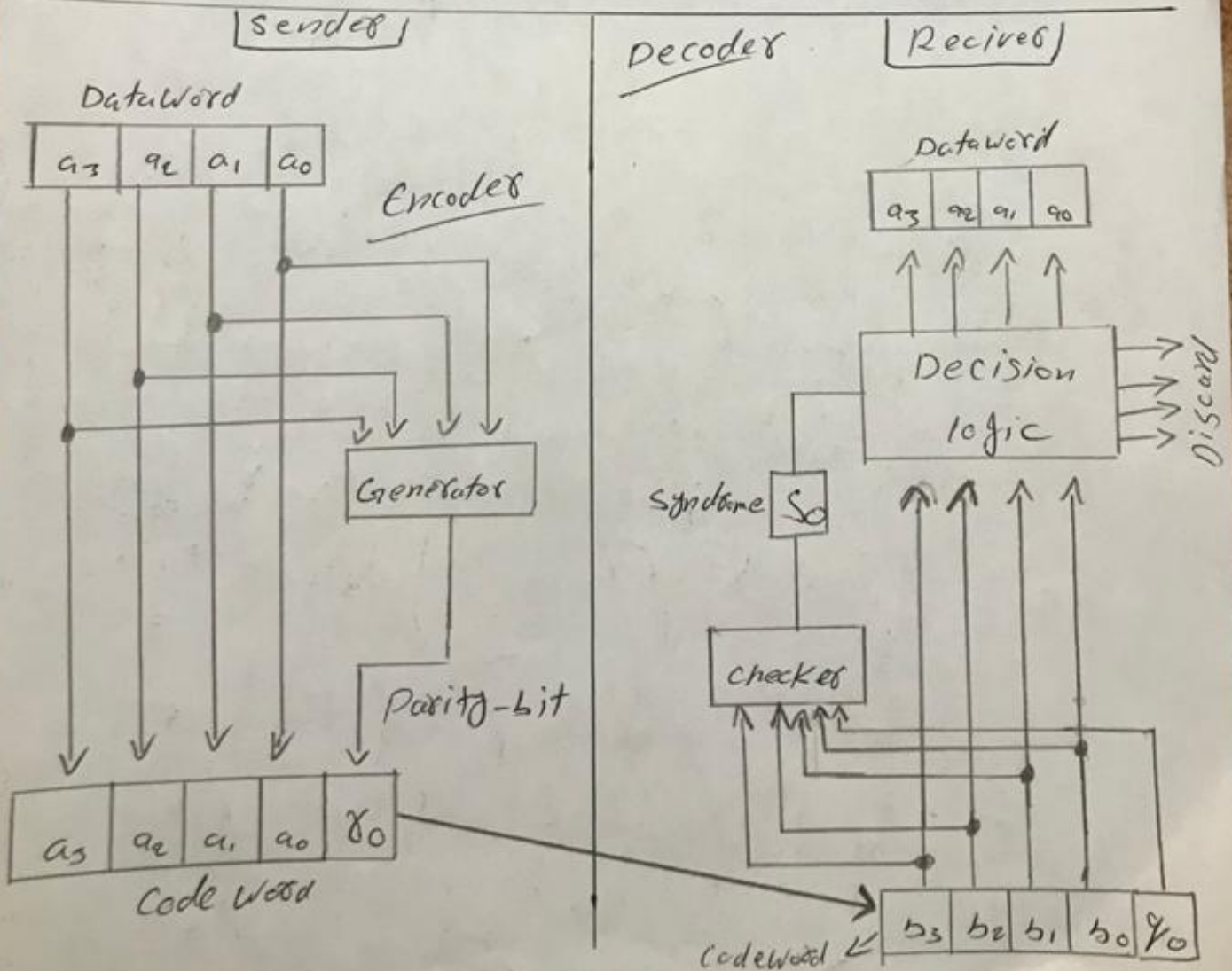
(B) simple parity-check code:

Ans The simple-Parity-check code is the most familar error-detacting code. In this code, ~~a k-Bit~~ a k-Bit data word is changed to an n-bit code word where $n = k+$.

1) The extra Bit called parity bit, is selected to make the total number of

Is in the code word even. Although some implementation specify an odd number of 1s. The minimum Hamming distance for the category is $d_{min} = 2$, which means that the code is a single-bit error detection code and it cannot correct any error.

(2) Simply parity checkcode diagram.



Q = 4

Ans The Lower limit of The supply voltages depends on The sum of The Threshhold voltage of The n-mos inverter & VDD.

OR

The inverter have always lower limit of The power depends on The sum of The Threshold V of The nmos & VDD.

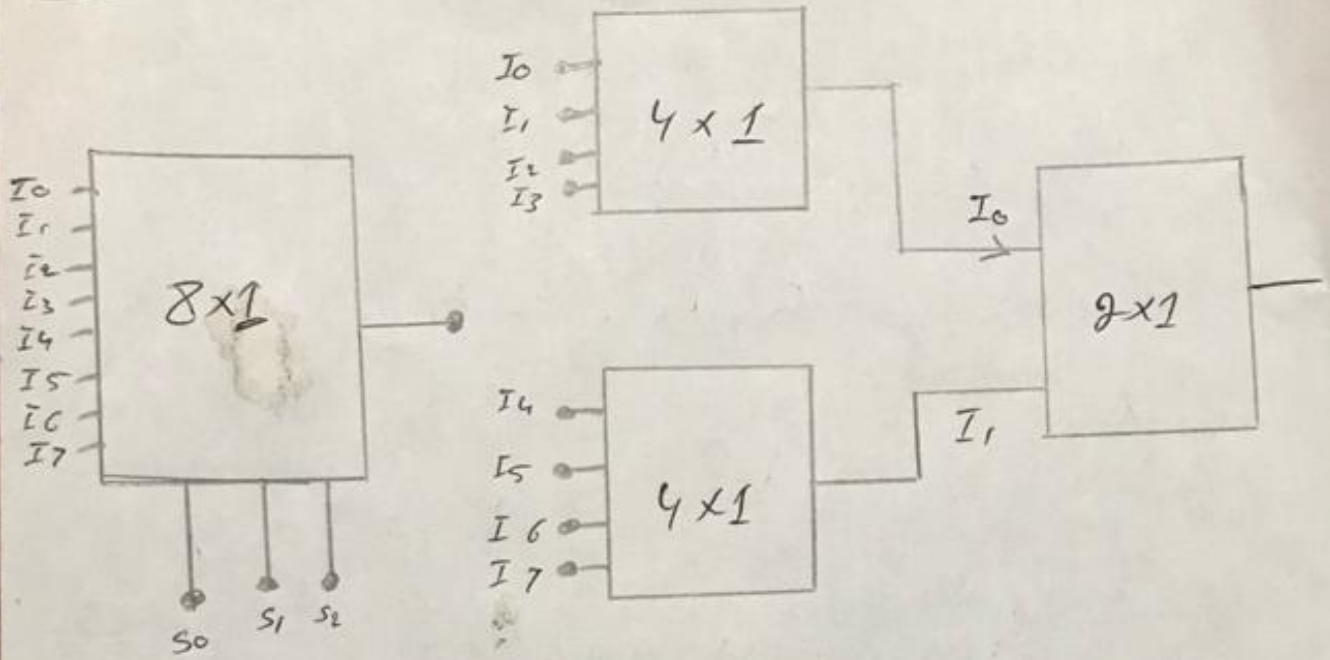
(a) Logic function is implemented by Pull-down network only.

(b) Full swing outputs (VOL = GND & VOH = VDD)

(c) Non-ratioed

(d) Faster switching speeds.

Q=5



8 x 1

Truth Table

S2	S1	S0	output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

P - T - O

M-Usama 9 14150

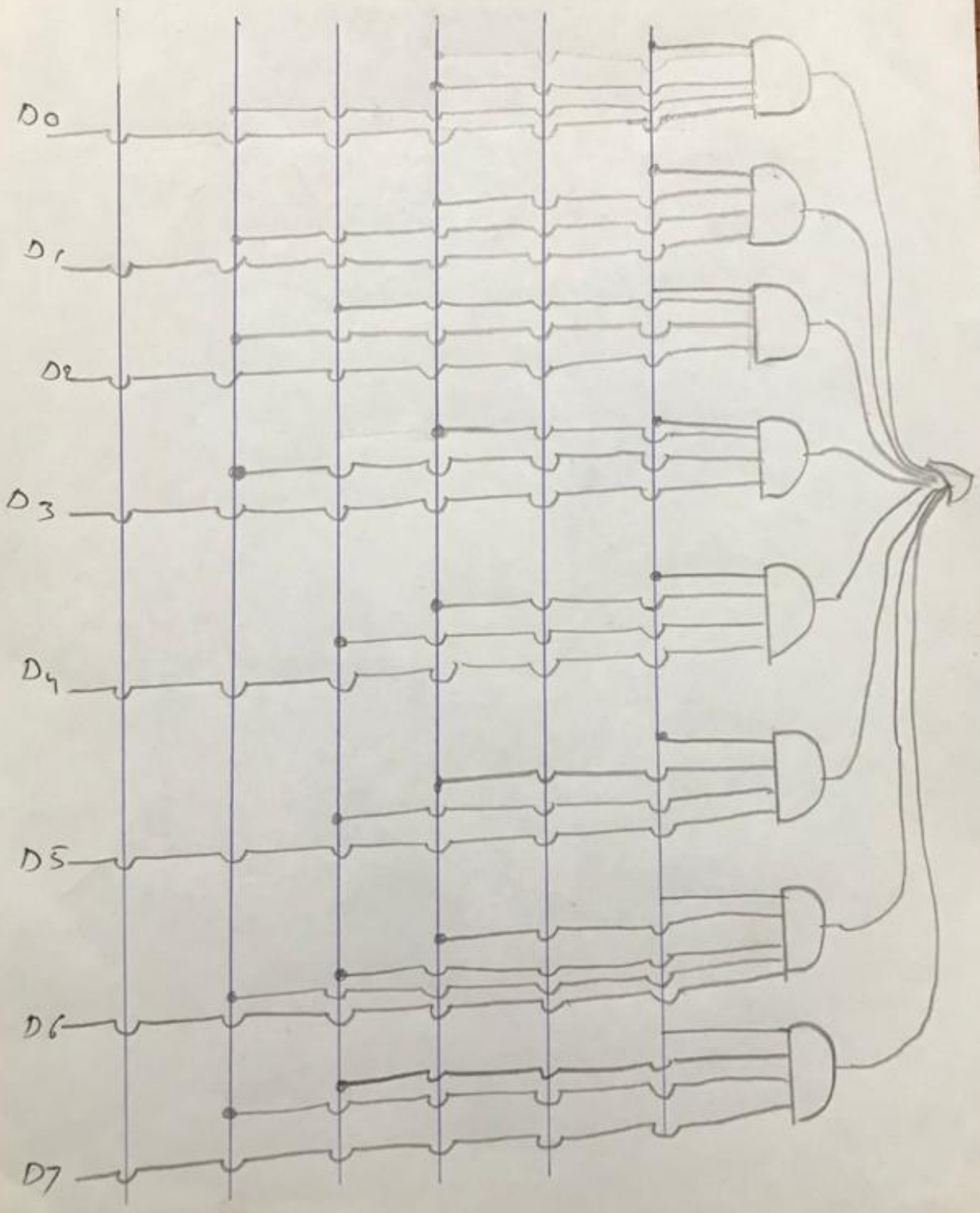
4 x 1

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2 x 1

S_1	S_0	Y
0	0	I_0
0	1	I_1

M. Usama 10 1450



M.Usama || 14150

8 x 1 Mux by VD. Method

$I_0 = S_2 \bar{S}_1 \bar{S}_0$

$I_1 = \bar{S}_2 \bar{S}_1 S_0$

$I_2 = \bar{S}_2 S_1 \bar{S}_0$

$I_3 = \bar{S}_2 S_1 S_0$

$I_4 = S_2 \bar{S}_1 \bar{S}_0$

$I_5 = S_2 \bar{S}_1 S_0$

$I_6 = S_2 S_1 \bar{S}_0$

$I_7 = S_2 S_1 S_0$