Name: Hamid Pir

ID: 6961

Paper: Computer Architecture.

1.

Give answers to each of the following:

a. Discuss the techniques used in contemporary processors to increase speed?

Ans: The techniques used in contemporary processors to increase speed are following:

* **Pipelining:-**

Pipelining enables a processor to work simultaneously on multiple instructions at the same time

* **Branch prediction-**

Branch prediction potentially increases the amount of work available for the processor to execute.

* **Superscalar Execution-**

This is the ability to issue more than one instruction in every processor clock cycle. In effect, multiple parallel pipelines are used.

*. **Data flow analysis:-**

The processor analyzes which instructions are dependent on each other's results, or data, to create an optimized schedule of instructions.

*. **Speculative Execution:-**

This enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

b. Discuss the speedup of program using multiple processors compared to a single processor using Amdahl's law?

Ans: The speedup using a parallel processor with N processors that fully exploits the parallel portion of the program is as follows.

Speedup = Time to execute program

on a single processor/Time to execute program on N parallel processors

$$= T(1-f) + Tf/T(1-f) + Tf/N = 1/(1-f) + f/N$$

C. Discuss the quickpath Interconnect protocol layers?

Ans: In the layer the packet is defined as the unit of transfer. One key function performed at this level is a cache coherency protocol, which deals with ensuring that main memory values held in multiple cache are consistent. A typical data packet payload is a block of data being send to or from a cache

a doubling every 18 months in the 1970's but has subdained that rate since

1. the cost of computer.
2. the electrical path length is shortened increasing speeding.
3. the computer becomes smaller
4. there are a reduction power requirements.
5. there are power tricechip connections.

6. Cycle state diagram:-

Instruction fetch

Read instruction from its memory location into the processor.

Instruction operation Decoding:-
Analyse instruction to determine

d. Discuss the physical and logical architecture of PCIe in detail?

Ans: A typical computer device also referred to as a chipset or a host bridge connects the processor and memory subsystems to the PCI express switch fabric comprising one or more PCIe end PCIe switch and PCIe switch devices.

Q2. Write a note on each of the following:

a. Consequences of Moore's law.

Moore's Law-

Gordon Moore observed that the number of transistors was doubling every year on a single chip. The pace slowed to

* Explain
one designed to perform parallel operations on graphic data it is used to execute and render 3D and 2D graphic as well as processes

Ans:
(a) Discuss the IR operation using the flowchart in details?

Sol:
the IR operates by respectively performing an instruction cycle. Each instruction cycle consists of three sub cycles.

1. Fetch Cycle:
the operands of next instruction is loaded from the IR and

Type of operations to be performed and operands(s) to be used.

c. Key characteristics of family C?

Similar or Identical Instructions Set:

This means that programs can grow up but not down.

Identical Operating System:

The same basic OS is available for all family members.

Increasing speed:

The rate of instruction execution increases in going from lower to higher family members.

d. Classes of Interrupts:

Programs:

It is generated by some exception that occurs as a result of an "instruction execution. Such as arithmatic overflow division by zero or reference outside a users allowed memory space.

Hardware failure :-

It is generated by a failure such as power failure or memory parity error.

Q:- Differentiate each of the following?

a. Cortex-A, Cortex-R, and cortex-M:-

Cortex-A:-

The cortex A and cortex A50 are application processors intended for mobile devices such as smartphones and E book readers digital TV home gateway etc.

Cortex R:-

The cortex R is designed to support real time application in which the time of event need to be controlled with rapid response to events they occur at a high frequency.

e.g ⇒ 200 MHz to 800 MHz.

Cortex M8-

Cortex M1 device processors have been developed primarily for the microcontroller domain where the need for fast highly deterministic interrupt response is coupled with the desire for extremely low gate count and lowest possible power consumption.

b. Disable interrupt and nested interrupt processing?

*. Disable interrupts:-

Simply ensure that the processor can and will ignore that interrupt request signal.

Nested Interrupt:-

ability to allow an interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted.

C. Multicore MIC and GPGPU?

*. Multicores-

The use of multiple processor on the same chip provides the potential to increase performance without increasing the clock rate.

*. MIC:-

Leap in performance as well as the challenges in developing software to exploit such a large number of core

the addresses portion is loaded into the MAR. This instruction perhaps taken from the IBR.

2. Execute Cycle:-
The control circuitry interprets the opcode and executes the instructions by sending out the appropriate control signal to cause data to be moved or an operation to be performed by the ALU.

a. Figure 01 shows the IBM enterprise EC12 core layout. Briefly explain the function of each sub area?

* IDU (Instruction decode Unit).
IDU is responsible for the parsing and decoding of all ZI architecture operation codes

*. LSU:- (Load Store Unit).
It is responsible for handling all Type of operands access of all basic modes and formats.

*. XU:-
It is unit translate logical address from instruction into physical address in the main memory.

*. FXU:- (Fine point Unit).

Q5

(a) A [illegible]

Ans:

Instruction Type	Instruction Count	Cycles Per Instruction
[illegible]	[illegible]	1
[illegible]	[illegible]	2
[illegible]	[illegible]	2
[illegible]	[illegible]	2

Ans:

Effective CPI:

CPI = (1*[illegible]) + (2*[illegible]) + (2*[illegible]) + (2*[illegible]) / [illegible]

CPI = 1620000/1000

CPI = 1620

MIPS Rate:

MIPS Rate = 60 MHz / 1620 * [illegible]