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**Question no :1**

**Answer:**

**Part (a):**

 

**Part (b):**

**Question no # 02:**

**Answer:**

**Collector curves:**

A family of collector characteristic curves is produced when IC versus VCE is plotted for several values of IB . When IB = 0, the transistor is in the cutoff region although there is a very small collector leakage current as indicated. Cutoff is the non-conducting state of a transistor.

Now we draw a collector curves BJT transistor.



**Region of operation:**

There are four region of operation, we discuss below

 **Active region:**

The curve has different regions where the action of a transistor changes. First, there is the region in the middle where Vce is between 1 and 40V. This represent the normal operation of a transistor. In this region, the emitter is forward biased, and the collector diode is reversed biased. Furthermore, the collector is almost gathering all the electron that the emitter has sent into the base. This is why changes in collector voltage have non- effect on the collector current. This region is called active region.

**Breakdown region:**

Another region of operation is the breakdown region. The transistor should never operate in this region because it will be destroyed. Similarly zener diode, which is optimized for breakdown operation, a transistor is not intended for operation in the breakdown region.

**Saturation region:**

Saturation region is one in which both Emitter Base and Base Collector junctions of the transistor are forward biased. In this region high currents flows through the transistor, as both junctions of the transistor are forward biased and bulk resistance offered is very much less. Transistor in saturation region is considered as on state in digital logic.

A transistor is said to be in saturation if and only ifβ >Ic /Ib. This is due to the fact that as both junctions of transistor are forward biased along with electron current flowing from emitter to base in active region there will be additional component of electron current flowing from collector to base. Small changes in collector to base forward voltage leads to large variations in collector currents (variations in currents will be exponential as mentioned before through diode current equation).

**Cuttoff region:**

A four possible region of operation. That the base current is zero, but these still is a small collector current. On a curve tracer, this current is usually so small that you cannot see it. We have exaggerated the bottom curve by drawing it larger than usual. This bottom curve is called the Cutoff region of the transistor and the small collector current is called the collector cutoff current.

**Question no 3:**

**Answer:**

**Transistor configuration:**

Transistor circuits use one of three transistor configurations: common base, common collector (emitter follower) and common emitter - one is selected during the electronic circuit design process.

The three different transistor circuits configurations are which is common emitter, common base and common collector emitter follower, these three circuit configurations have different characteristics and one type will be chosen for a circuit dependent upon what is required.

**Common base configuration:**

This is the first transistor configuration, which we want to discuss here, This transistor configuration provides a low input impedance while offering a high output impedance. Although the voltage is high, the current gain is low and the overall power gain is also low when compared to the other transistor configurations available. This transistor configuration is probably the least used, but it does provide advantages that the base which is common to input and output is grounded and this has advantages in reducing useless feedback between output and input for different RF circuit design applications. This occurs because the base, which is the electrode physically between the emitter and collector is grounded, thereby providing a barrier between the two. As a result, the common base configuration tends to be used for RF amplifiers where the increased isolation between input and output gives a greater level of stability and reduces the likelihood of unwanted oscillation.



**Common Collector Configuration:**

This is the second configuration of transistor, in common collector circuit configuration is possibly more widely known as the emitter follower because the emitter voltage follows that of the base, although lower in voltage by an amount equal to the turn on voltage of the base emitter junction. The common collector, emitter follower offers a high input impedance and a low output impedance. The voltage gain is unity, although current gain is high. The input and output signals are in phase. in this transistor configuration, the collector electrode is common to both input and output circuits. Now we draw figure



**Common Emitter configuration:**

It is another configuration of transistor in which the circuit provides a medium input and output impedance levels. Both current and voltage gain can be described as medium, but the output is the inverse of the input, i.e. 180° phase change. This provides a good overall performance and as such it is often the most widely used configuration.

**Question no # 4:**

**Answer:**

**E-MOSFET:**

E-MOSFET can be classed as normally off (non-conducting) devices, that is they only conduct when a suitable gates to source positive voltage is applied, unlike depletion type mosfet which are normally on devices conducted when the voltage is zero.

**P and N region:**

 we can control how the mosfet operates by creating or “enhancing” its conductive channel between the source and drain regions producing a type of mosfet commonly called an n-channel Enhancement-mode MOSFET, which simply means that unless we bias them positively on the gate (negatively for the p-channel), no channel current will flow.

There are large variations in the characteristics of different types of mosfets, and hence the biasing of a mosfet must be done individually. As with the bipolar transistor common emitter configuration, the common source mosfet amplifier needs to be biased at a suitable quiescent value. But first let’s remind ourselves of the mosfets basic characteristics and configuration.

 **N-channel E-MOSFET:**

The MOSFET differs from the BJT in that there is no direct connection between the gate and channel, We can see that for the n-channel MOSFET (NMOS), above the substrate semiconductor material is p -type, while the source and drain electrodes are n-type. The supply voltage will be positive. Biasing the gate terminal positive attracts electrons within the p-type semiconductor substrate under the gate region towards it. This overabundance of free electrons within the p-type substrate causes a conductive channel to appear or grow as the electrical properties of the p-type region invert, effectively changing the p-type substrate into a n-type material allowing channel current to flow.

The reverse is also true for the p-channel MOSFET , where a negative gate potential causes a build of holes under the gate region as they are attracted to the electrons on the outer side of the metal gate electrode. The result is that the n-type substrate creates a p-type conductive channel.

So for our n-type MOS transistor, the more positive potential we put on the gate the greater the build-up of electrons around the gate region and the wider the conductive channel becomes. This enhances the electron flow through the channel allowing more channel current to flow from drain to source leading to the name of  e-mosfet.

**E-Mosfet amplifier:**

Due to the construction and physics of an enhancement type mosfet , there is a minimum gate-to-source voltage, called the threshold voltage VTH that must be applied to the gate before it starts to conduct allowing drain current to flow.

In other words, an enhancement mosfet does not conduct when the gate-source voltage, VGS is less than the threshold voltage, VTH but as the gates forward bias increases, the drain current, ID (also known as drain-source current IDS) will also increase, similar to a bipolar transistor, making the eMOSFET ideal for use in mosfet amplifier circuits. The fundamental of the MOS conductive channel can be thought of as a variable resistor that is controlled by the gate. Drain current amount is flow through this n-channel therefore depends on the gate-source voltage and one of the many measurements we can take using a mosfet is to plot a transfer characteristics graph to show the i-v relationship between the drain current and the gate voltage as shown.



**Question No#5:**

**Answer:**

**Part (a):**

**Advantage of BJT:**

The main advantage of BJTs are that they have faster switching speeds and higher operating frequencies. BJTs historically have had greater power handling capabilities than FETs, but the power handling ability of MOSFETs has improved since their first introduction , particularly with the development of devices called “VMOSFETs”.

**Disadvantages of BJTs:**

* The fact that they are current driven means they consume more power and also generate more waste heat, (some components such as microprocessors require cooling when they are in use).
* The heat generated, limits how closely BJTs can be packed onto integrated circuits, (they need more spacing to dissipate then heat, so you can fit as many BJTs on an IC, compared to FETs.

**Advantage of FETs:**

* They can be used to amplify low power signals( the signal don’t neet to expend energy to control the gate).
* They present very high impedance, so measuring instruments based on FETs don’t load the circuits they are connected to.
* The4y can result in long battery life for portable devices.
* The low current consumption and therefore low heat generation enables denser packing of FETs in integrated circuits.

**Disadvantages of FETS:**

it include slower switching speed and lower frequency limits compared to BJTs. One particularly important aspect with MOSFETs that requires caution, is that static electricity van destroy or damage the thin insulation between the gate and substrate. Therefore handling precautions are required to eliminate static electricity.

**Part (b):**

**Answer:**

When the drain voltage is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential and the channel. The channel inversion layer change decreases with increases drain –source voltage and ultimately, it becomes zero when the drain –source voltage equals to (Vgs-Vgs(th)) . This point is called the channel pinch-off voltage where the drain current becomes saturated.