Assignment no 4.

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BS(CS) 4th

Q1

→ Relation among access time, memory cost, capacity:-

→ As access time becomes faster, the cost per bit increases, As memory size increases the cost per bit is smaller, Also with great capacity the access time becomes slowel.

(2)

→ Diff Memory Access methods:

→ Sequential Access :- Sequential access is accessing data in a specific linear sequence.
example :- Tape storage.

→ Direct Access :- Direct access has the data address being based on a physical location.

→ Random Access :- With random access every any location can be selected at random, and the addressable locations in the memory have a unique, physically wired-in addressing mech

→ Set Associative is an enhanced form of the direct mapping, where drawbacks of direct mapping have been taken out.

→ It allows each word in cache can have 2 or more words in main memory.

(3)

→ Split Cache & Unified Cache :-

→ A split cache is a cache that consists of two physically seperated paths, where one part called the instruction cache is dedicated for holding instructions and the other called the data cache is dedicated for holding data

→ A unified cache is a cache which holds data and instructions in the same cache.
→ It reduces contention for memory b/w intruction and data access.

Q2.

(1)

→ Memory Unit of Transfer :-

→ Data Transfer, the rate at which digital data can be transfered from one storage device to another.

→. Weather these devices are connected to the same machine or through a network.

→ Transfer units are represented by unit of digital data divided by unit of time.

→ Memory Pierformance Parameters :-

→ The performance parameters defins the processing time of the memory cache and the operational batch sizes.

→ If you exceed the available memory with excessively large cache, performance will severely degrade. However an inadequately sized cache will result in similar poor performance from excessive CPU & disk utilization

→ Cache Memo Parameters :-

The cache memory defines the object cache settings to optimize system response time and throughput of Runtime objects.

→ Disk Cache :-

A disk cache is a mechanism for improving the time it takes to read from or write to a hard disk.

→ The disk cache is usually included as part of the hard disk.

→ A disk cache can also be a specific portion of RAM.

→ Its purpose is to act as temporary memory for the hard drive as it reads and writes data to the permenant storage on the platters.

→ Principal of Locality :-

→ "Data in the vincity of a refrenced word are likely to be referenced in the near future".

→ Logical cache & physical cache :-

→ A logical cache stores data in a virtual address space.
→ A logical cache is located b/w the processor and MMU.

→ A physical cache stores memory using physical addresses.
→ It is located b/w MMU & main memory.

→ Possible Approaches to the cache coherency :-

→ Hardware transperency is used to see if all updates to main memo via cache are reflected in all cache.

→ Thus if one processor modifies a word in its cache. this update is written to main memory.

→ Non-Cacheable Memory :-

A small portion of main memory is shared by more processors and it is non-cacheable.

→ The non cacheable memory can be identified using chip select logic or high address bits.

(Q3)

→ Differenciate following :-

(1)

→ Seq Access, Direct Access, Random Access :-

→ Seq Access is accessing data in a specific linear sequence.
→ Direct access has the data address being based on a physical location.
→ Random Access is accessing any location randomly and address locations have unique addressing mechanism.

(2)

→ Direct, Associative, set-Associative mapping :-

→ Direct mapping is an inexpensive method to implement.
→ It maps each block into a possible cache line.
→ With Associative mapping, there is a flexibility as to which block to replace as to which block to be addressed to the cache.

→ Main Memo Addressing in Direct Maping :-
→ Maps each block into a possible cache line
→ no of blocks in main memory =
$2^{s+w}/2^{w} = 2^{s}$

→ Associative Mapping :-
→ A mein memory block can be loaded into any line of cache.
no of blocks in main memory =
$2^{s+w}/2^{w} = 2^{s}$

→ Set Associative :-
→ This form of mapping is enhanced from of direct mapping where drawbacks of direct mapping are removed.

→ Set associative mapping allows that each word that is present in the cache can have 2 or more words in main memory for same index address

$m = v * k$
$i = j \bmod v$
i = cache set number
j = main memory block.

(4)

→ Write back & Write through :-

→ Write back is a storage method in which data is written into the cache everytime a change occurs, but it is written into the corresponding location in the memory only at specified intervals or under certain conditions

→ In writethrough storage method the main memory data always stays fresh.

(Q4)

(1)

→ $(0.95)(0.01\ ms) + (0.05)(0.01\ ms + 0.1\ ms) =$

$0.0095 + 0.0055 = 0.015\ ms.$

The average access time is much closer to 0.01 ms than to 0.1 ms.