Programs: BC (CS), BS(SE), BS(TELC)

Subject: Digital Logic Design

Major Assignment Final-Term

Course Code: CSC-201

EDP Code: 102007016

Summer Semester 2020

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Q.1 Draw and explain the logic diagram for each of the following:

a) A circuit for adding or subtracting two 4-bit numbers

b) 4-bit active low decoder

c) Decimal to BCD encoder

d) Frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)

Q.2 For the 4-input multiplexer, data inputs are given as:

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find the output Y if the select inputs are given as:

a) $S_0 = 1$, $S_1 = 0$

b) $S_0 = 0$, $S_1 = 1$

c) $S_0 = 1$, $S_1 = 1$

d) $S_0 = 0$, $S_1 = 0$

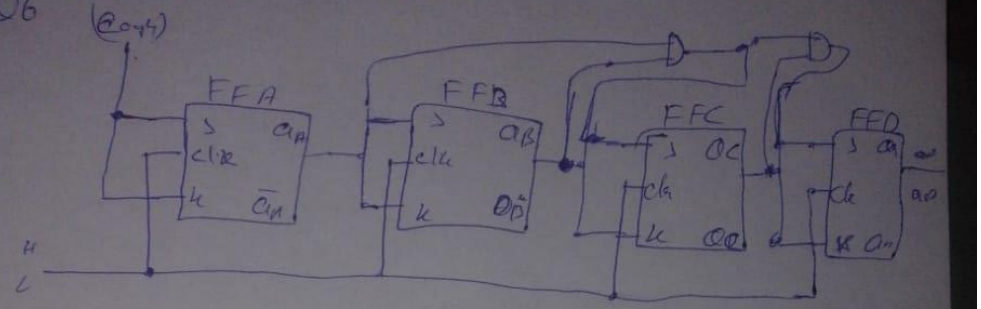
Q.3 Timing diagram in Figure 01 shows inputs to a 9-bit parity checker. Draw the ∑ Even and ∑ Odd output for the even parity checking.

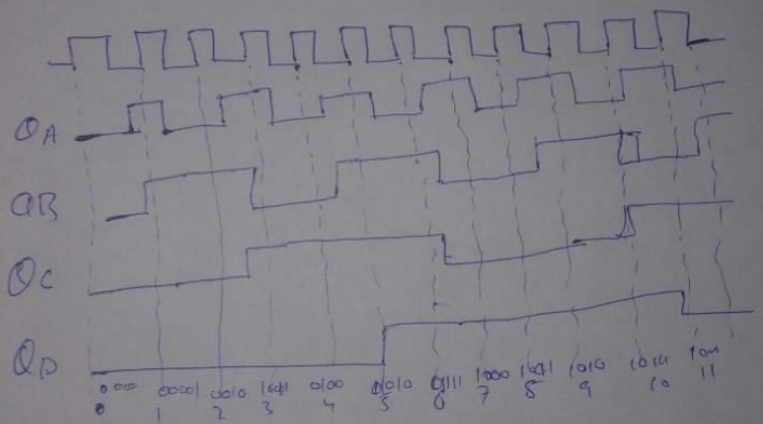
Q.4 The waveforms in Figure 02 are applied to the J, K, CLK, $\overline{PRE}$, and $\overline{CLR}$ inputs as indicated. Determine the Q output, if the flip-flop is initially RESET.

Q.5 Use the waveforms in Figure 03 to draw the timing diagram for the parallel outputs(Q_1, Q_2, Q_3, Q_4) for the shift register. Assume that register is initially cleared.

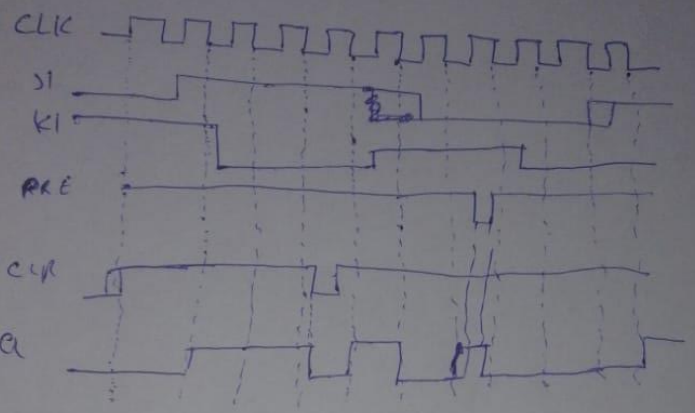
Q.6 Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

Q6





(1) (4)



Note the each case is applied to the IRRE, the flip-flop is set or reset regardless to the state to other input.

Q2

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$ $D_3 = 1$

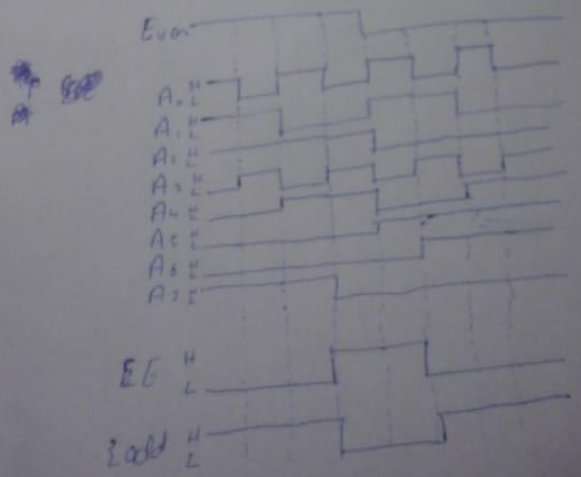
a) = $S_0 = 1$, $S_1 = 0$ $Y = 0$

b = $S_0 = 0$, $S_1 = 1$ $y = 1$

c) $S_0 = 1$ $S_1 = 1$ $Y = 0$

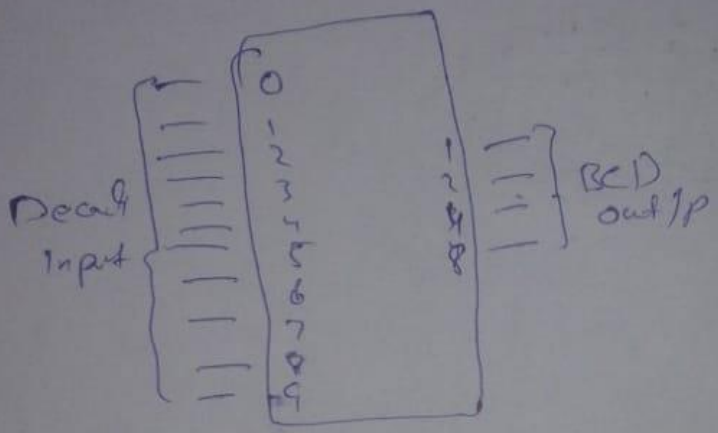
d) $S_0 = 0$ $S_1 = 0$ $Y = 1$ (Ans)

Q3



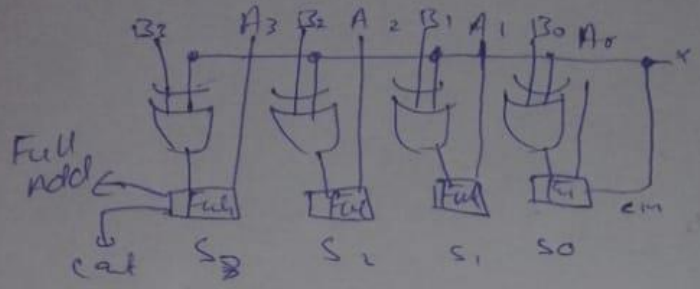
(c)

encoda has ten inputs - one for each derival digit and 7or outputs the output indicat the BCD code that reperal the actul input.

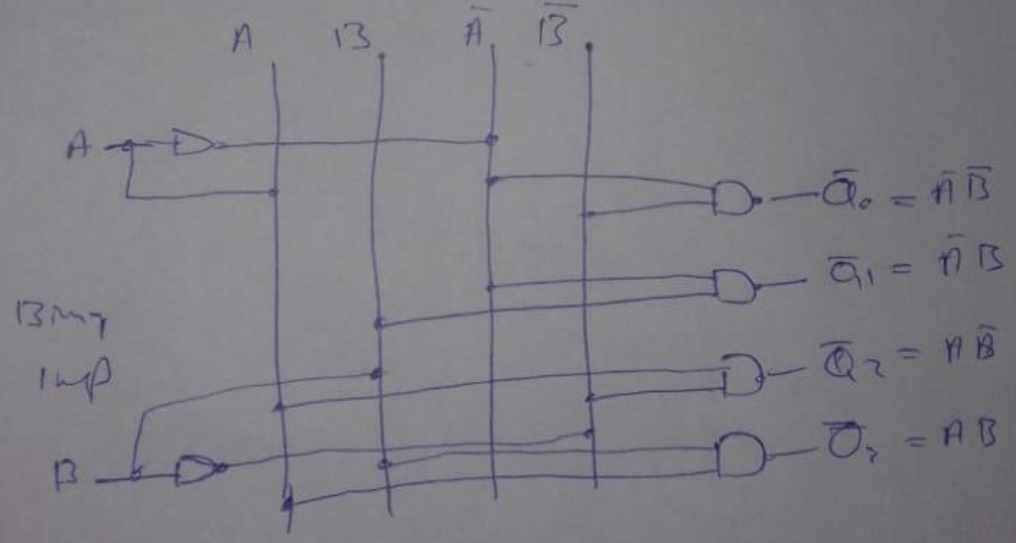


Q1

(a) (i) In Digital Circuit, A binary adder subtractor is one which is capable of both addition and subtraction of binary number is one circuit it is also it is one of the component of ALU



(b)



A B	a_0	a_1	a_2	a_3
0 0	0	1	1	1
0 1	1	0	1	1
1 0	1	1	0	1
1 1	1	1	1	0