Department of Electrical Engineering
Mid-term
Date: 24/08/2020

Course Details

Course Title: Electronic Circuit Design **Module:** _____
Instructor: _____ **Total Marks:** 30

Student Details

Name: **Shehriyar khan** **Student ID:** **13738**

Student Signature: _____

Q1.		For the circuit given in figure 1. Answer the following: a) Which type of transistor is that? b) Label the Drain, Source and Gate. c) Determine the values of V_{DS} and V_{GS}	Marks 09

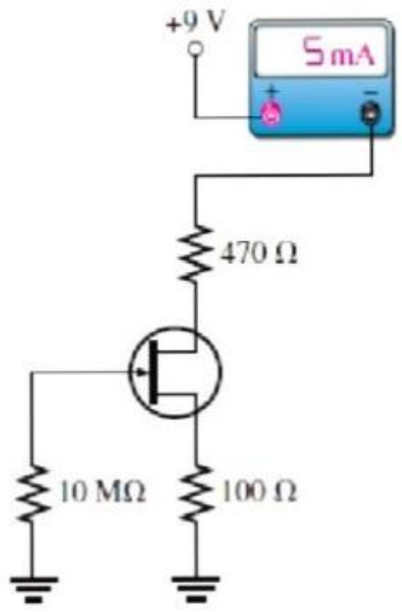

Figure 1

Q2.		**Explain** the drain characteristic curve of D-MOSFET given below in Fig. 2.	Marks 06

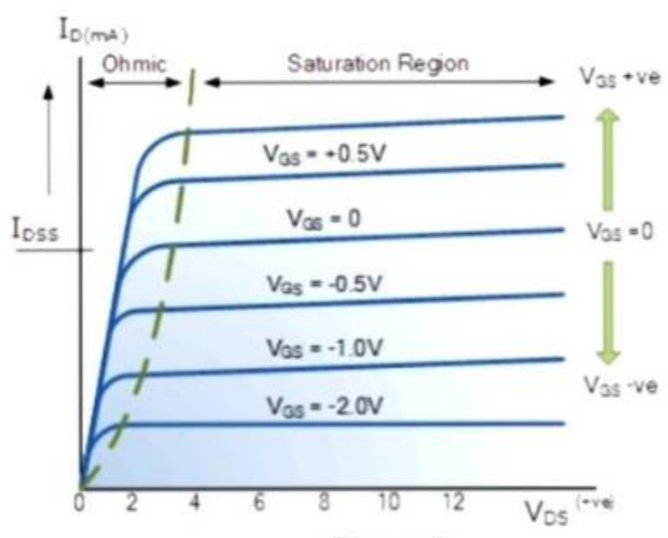

Figure 2

Q3.		**Sketch** the hybrid equivalent for common emitter transistor. Write equations for the transistor in common emitter configuration.	Marks 05
Q4.		**Explain** why both types of MOSFETs have an extremely high input resistance at the gate. (Marks 01) In **what** mode an *n*-channel D-MOSFET with a positive *V*GS is operating? (Marks 01) **Why** must the gate-to-source voltage of an *n*-channel JFET always be either 0 or negative? (Marks 01) **Briefly discuss** that how BJT differs from FET? (Marks 04) MOSFET is also called IGFET, give reason **why**? (Marks 01) **Why** JFET is called Squared Law Device? (Marks 01) **What** can be the main disadvantage of common-base amplifier as compared to the common-emitter and emitter-follower amplifiers? (Marks 01)	Marks 10

Name Shehriyar Khan

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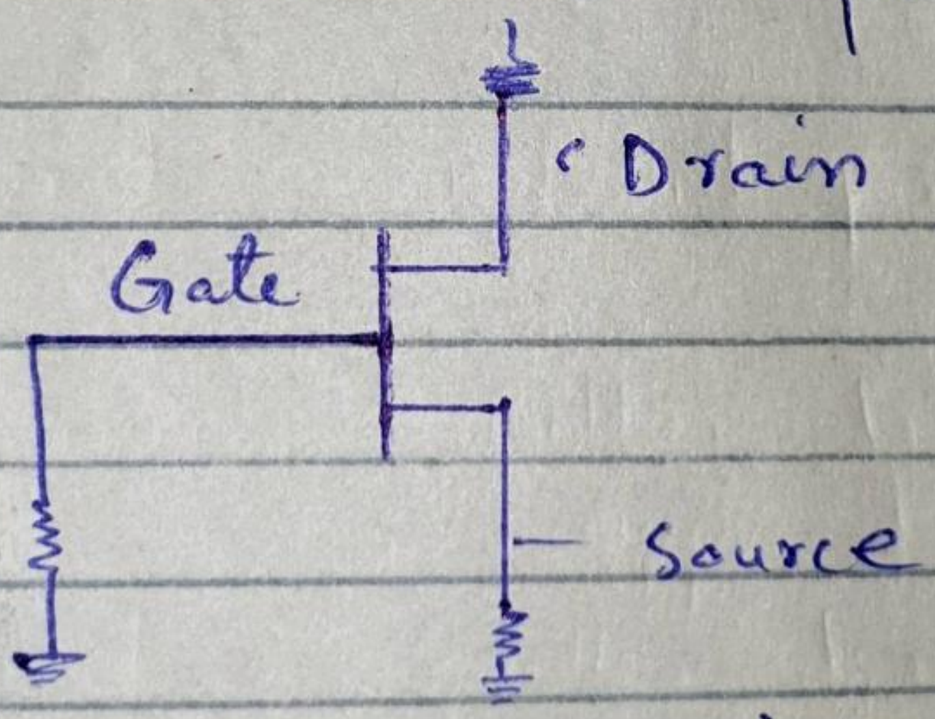
BE (Electrical).

GNO(1)

(a) This is a pNP Transistor.

(b)



(c) $V_S = (5\text{mA})(100\Omega) = 0.5\text{V}$

$V_D = 9V - (5\text{mA})(470\Omega) = 6.65\text{V}$

$V_G = 0V$

$V_{GS} = V_G - V_S = 0V - 0.5\text{V} = -0.5\text{V}$

$V_{DS} = V_D - V_S = 6.65 - 0.5 = 6.15\text{V}$

Q2:-

Answer: Depletion Mode: The depletion Mode MOSFETS are generally known as Switched ON, device because these transistor are generally closed when there is no bias ~~voltat~~ voltage at the gate terminal of the gate voltage increases in positive, then the channel width increases in depletion mode.

characteristis of curve of Depletion Mode MOSFET:

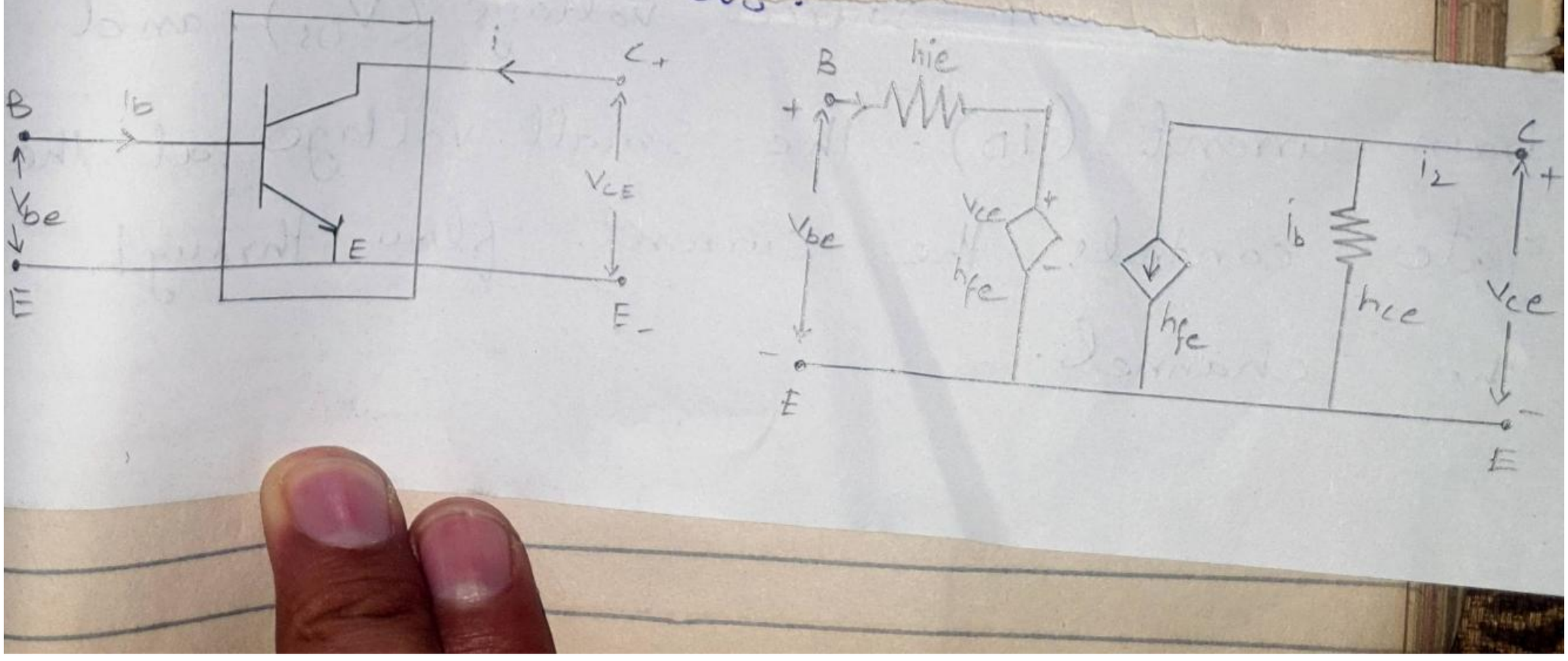
The characteristis of the depletion Mode MOSFET transistor are give above. This characteristis mainly gives the relationship between drain-Source voltage (V_{DS}) and drain current (ID). The small voltage at gate controls the current flow through the ~~cha~~ channel.

The channel between drain and source act as a good conductor with zero bias voltage at gate terminal. The channel width and drain current. increases if gate voltage is positive and These TWO (channel width and drain current) decreases if the gate voltage is negative.

Q3)

Hybrid equivlent For CE Transistor:

In common emitter transistor configuration the input sigal applied b/w the base and emitter terminals of the transistor and output appears b/w the collector and emitter terminals.



The input voltage (Vbe) and output current (Ic) are give by the following equation.

$$Vbe = hie \cdot ib + hre \cdot Vc$$
$$Ie = hfe \cdot Ib + hoe \cdot Vc$$

Q No (4):

MOSFETS have a very high input resistance because the gate is insulated from the channel by an SiO_2 layer

Q4(ii)

An n-channel D-MOSFET with a positive V_{GS} is operating in the enhancement mode.

Q4(iii)

The gate to Source voltage of an n-channel JFET must be zero or negative in order to maintain the required reverse bias condition

Q No 4(iv)

Differance b/w BJT and FET :-

(1) BJT is a Bi polar junction transistor.

In this transistor there is a

flow of both majorty and charge carries.

While FET are uniplar. only flow on majority charge carriers.

ii) BJTs are current controlled FET are voltage controlled.

iii) BJTs consist of three terminals namely emitter, Base, and collector.

FETs consist of three terminal namely source drain and gate.

(iV) BJTs have a higher max frequancy and a higher cutoff frquancy.

FETS have low to mediam gain.

Q No(4)

MOSFET called IGFET because metal oxide (The MO Part of MOSFET) is an insulator that sparates the gate etectrode from the body of the field effect transistor.

Q No 4 (vii)

(1) The input output - tranfer characteristics of the JFET is not as straight forward as it is for the BJT.

(2) In a BJT, B (h_{FE}) defined the relationship b/w IB (Input current) and IC (output current)

(3) In a JFET the relation b/w VGS and ID is used to define the transfer characteristis

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)$$

(4) As a result FET's are reffered to a square law device

Q NO 4 (viii)

In the common base amplifier configuration the input current exceeds all other currents in the circite, including the out put current. the current gain of this amplifier is actually less then 1.