# Assignment: 2

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Course: Computer Architecture

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# Q.1 Give answer to each of the following

# Ans: A

1 Image Processing: A microprocessor-based system is described for data capture and analysis of dynamic for data foot pressure images. A run-length encoding video digitiser captures up to 32 frames at a rate of 25 Per Second and stores the data in memory

2- Tree-dimensional rendering: Three-dimensional (3D) Computer graphics hardware has emerged to become an integral part of mainstream desktop pc systems. The aim of this paper is to describe the 3D graphics architecture at a level accessible to the general Computational Science Community.

3-Video Conferencing: Requirements for video Conferencing: your checklist For Hardware and Software

4- Multimedia authoring: multimedia authoring systems for constructing Education packages for Special needs-

Education

**Ans: B** There are three approaches to achieving increased processor speed

1 Increased the hardware speed of the processor. This increased is fundamentally due to shrinking the size of the logic gate- Can be packed together more tightly and to increasing the clock rate.

2: Increase the size and speed of caches that are interposed between the processor and main memory. In particular, by dedicating a portion of the processor chip itself to the cache, cache access times drop significantly

3: Make changes to the processor organization and architecture that increase the effective speed of instruction execution

**Ans: C** Clock speed and logic density increase, a number of obstacles become more significant.

* Power: As the density of logic and the clock speed on a chip increase, so does the Power density (watts/$cm^2$).

* Rc delay: The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wires connecting them specifically, delay increases as the RC product increases as the RC Product increases.

* Memory latency and throughput: memory access speed and transfer speed through processor speeds. as previously discussed. However, simply relying on increasing clock rate for increased performance runs into the power dissipation problem already refferred to.

## Ans D:

Amdahl's law was first Proposed by Gene Amdahl in 1967 and deal with the Potential speedup of a program using multiple processors compared to a single processor. Consider a program running on a single processor such that a fraction (1-F) of the execution time involves code that is inherently sequential and a fraction F that is inherently sequential

Let T be the total execution time of the program using a single processor. Then the speedup using a parallel processor with N processor that fully exploits the parallel portion of the program is a follow.

$$\text{Speedup} = \frac{\text{Time to execute program on a single processor}}{\text{Time to execute program on N parallel processors}}$$

$$= \frac{T(1-f) + Tf}{T(1-f) + \frac{Tf}{N}} = \frac{1}{(1-f) + \frac{f}{N}}$$

$$\text{Speedup} = \frac{1}{(1-f) + \frac{f}{\text{Sup}}}$$

**Q.2** Solve each of the following:

**Ans: A**

Calculating the CPI

$$CPI = \frac{\text{Instruction Count} \times \text{Cycles Per Second}}{\text{Number of instructions the executed Program consists}}$$

$$CPI = \frac{(146000 \times 1) + (33000 \times 2) + (16000 \times 2) + (9000 \times 2)}{104000}$$

$$= \frac{46000 + 66000 + 32000 + 18000}{104000}$$

$$= \frac{162000}{104000} = 1.557$$

Calculating MIPS

Processor Time $T = I_c \times CPI \times \tau$

$\tau$ represents Constant cycle time

$$\frac{1}{F}$$

$$MIPS = \frac{Ic}{T \times 10^6}$$

$$= \frac{Ic}{Ic \times CPI \times 2 \times 10^6} = \frac{1}{CPI \times \frac{1}{F} \times 10^6}$$

$$= \frac{F}{CPI \times 10^6}$$

frequency is given as 60 MHz substitute 60 for "F" in the above formula

$$MIPS = \frac{60 \times 10}{1.557 \times 10^6}$$

$$= \frac{60}{10557} = 38.535$$

Therefore the MIPS for this program is

**38.535**

Calculating Execution Time (T)

$T = Ic \times CPI \times 2$

Substitute the values 104000

$$T = \frac{104000 \times 1.557}{60 \times 10^6} = \frac{161928}{60000000}$$

$$= 0.002698 = \boxed{2,6988}$$

# Ans: B

$$CPI_A = \frac{\sum_i CPI_i \times I_i}{I_c} = \frac{(8\times1\times4\times3+2+4+4+3)\times10^6}{(8+4+2+4)\times10^6}$$

$$= \approx 2.22$$

$$MIPS_A = \frac{f}{CPI_A \times 10^6} = \frac{200\times10^6}{2.22\times10^6} = 90$$

$$CPU_A = \frac{I_c \times CPI_A}{f} = \frac{18\times10^6\times2.2}{200\times10^6} = 0.2s$$

$$CPU_B = \frac{\sum_i CPI_i \times I_i}{I_c} = \frac{(10\times1+8\times2+2\times4+4\times3)}{(10+8+2+4)}$$

$$CPI_B = \frac{\times10^6}{\times10^6} = \approx 1.92$$

$$MIPS_B = \frac{f}{CPI_B \times 10^6} = \frac{200\times10^6}{1.92\times10^6} = 104$$

$$CPU_B = \frac{I_c \times CPI_B}{f} = \frac{24\times10^6\times1.92}{200\times10^6}$$

$$= 0.235$$

# Ans: C

**a.** The MIPS rate could be computed as the following:

$$[(\text{MIPS rate})/10^6] = Ic/T$$

Thus that:

$$Ic = T \times [(\text{MIPS rate})/10^6]$$

Now by computing the ratio of the instruction count of the IBM RS/6000 to the VAX 11/780 which is

$$[x * 18]/[12x * 1] = 18x/12x = \boxed{1.5}$$

**b.** Regarding to the VAX 11/780, the

$$CPI = (5\,MHz)/(1\,MIPS) = \boxed{5}$$

Regarding to the IBM RS/6000, the

$$CPI = (25\,MHz)/(18\,MIPS) = \boxed{1.4}$$

# Ans: D

**a.** Since we have the same instruction mix, that mean the adelitional instructions for each task could be allocated appropriately between the instruction types. Therefore, the following table be gotten.

| Instruction Type | CPI | Instruction Mix |
|---|---|---|
| Arithemetic Logic | 1 | |
| Load/store with Cache hit | 2 | |
| Branch | 4 | |
| Memory reference with cache miss | 12 | |

The average CPI = (1 x 0.6) + (2 x 0.18) + (4 x 0.12) + (12 x 0.1) = 2.64 Therefore, the CPI has been increased since the time for memory access is also increased.

**b.** MIPS = 400/2.64 = 152 There is a corresponding drop in the MIPS rate.

**C.** The speedup factor equals to the ratio of the execution times. The execution time is calculated as the following

$T = Ic / (MIPS \times 10^6)$

for the one processor $T_1 = (2 \times 10^6) / (178 \times 10^6)$

$= 11 ms$

for the 8 processors: each processor execute 1/8 of the 2 milion instruction plus the 25,000

$$T_8 = \frac{\frac{2 \times 10^6}{8} + 0.025 \times 10^6}{152 \times 10^6} = 1.8 ms$$

Therefore we have

$$Speedup = \frac{11}{1.8} = 6.11$$

**d.** if it is supposed that the fraction of code, which is parallelizable is $f = 1$, then Amdahl's law decreases to $Speedup = N = 8$ Therefore the actual speedup is only about 75% of the theretical speedup.