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1ND) Give answers to each of the following.

a) Discuss the concept of word, addressable units, and unit of transfer for internal memories.

NS) Word:-

The 'natural' unit of organization of memory. The size of word is typically equal to the number of bits used to represent an integer and to the instruction lenghth.

- Addressable units:-

In some systems, the addressable unit is the word. However, many systems allow addressing at the byte level. In any case, $2^A = N$.

- Unit of transfer:-

For main memory, this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an adressable unit.

b) How least recently used (LRU) and least frequently used (LFU) replacement algorithms are implemented for a cache memory with two-way set associative mapping?

Ans Probably the most effective is least recently used (LRU): Replace that block in the set that has been in the cache longest with no reference to it. For Two way set associative, this is easily implemented. Each line includes a USE Bit. When a line is referenced, its USE bit is set to 1 and the use bit of the other line in that set is set to 0. When a block is to be read into the set, the line whose USE bit is 0 is used. Because we are assuming that more recently used memory locations are more likely to be referenced, LRU should give the best hit ratio. LRU is also relatively easy to implement for a fully associative cache. The cache mechanism maintains a separate list of indexes to all the lines in the cache. When the line is referenced, it moves to the front of the list. For replacement, the line at the back of the list is used. Because of its simplicity of implementation, LRU is the most popular replacement algorithm.

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Still another possibility is least frequently used (LFU): Replace that block in the set that has experienced the fewest references. LFU could be implemented by associating a counter with each line. A technique not based on usage is to pick a line at random from among the candidate lines. Simulation studies have shown that random replacement provides only slightly inferior performance to an algorithm based on usage [SMIT82].

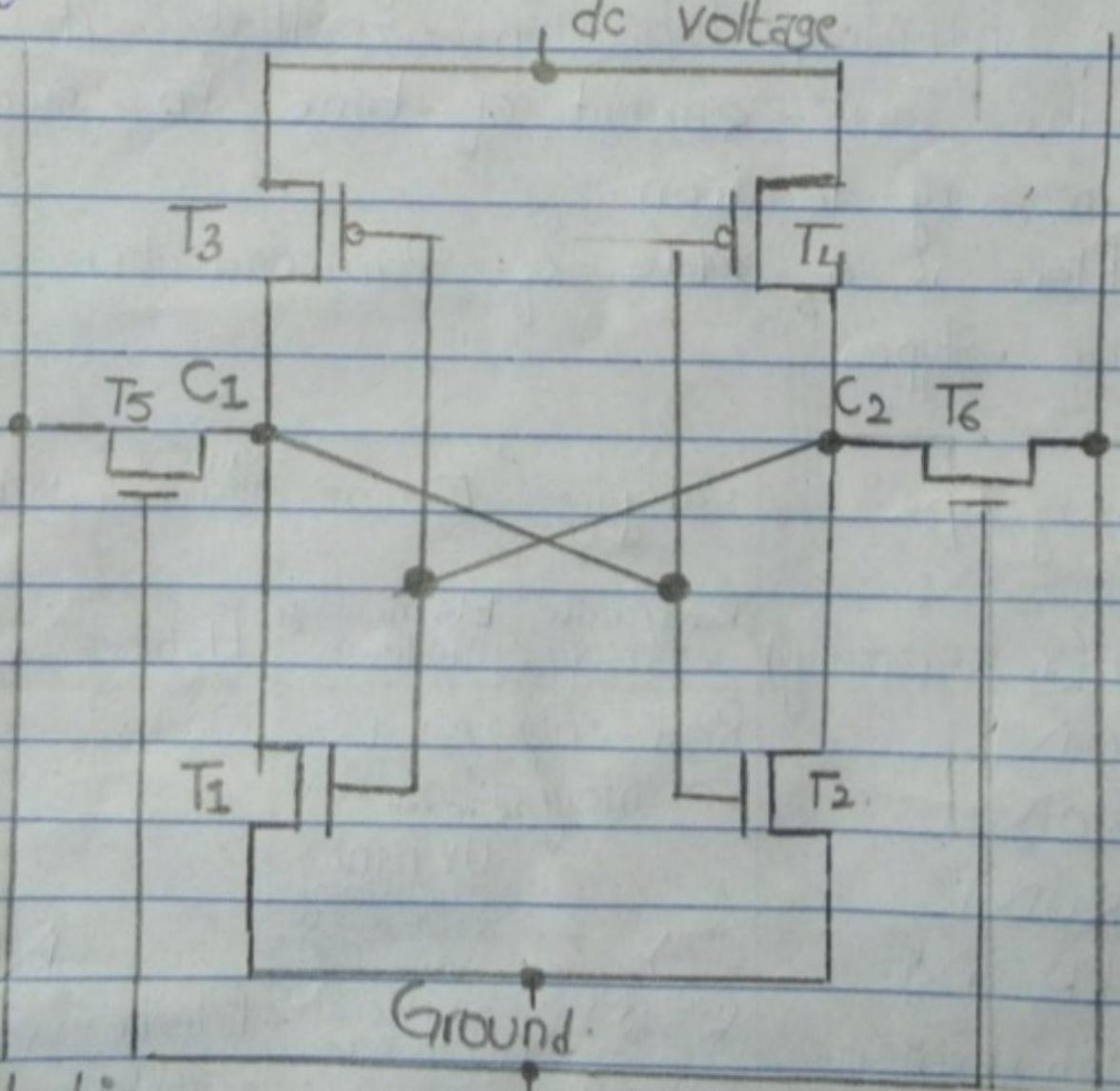
Explain the read and write operation for the SRAM cell using diagram.

Read operation:-

In SRAM, for any operation to be performed, the word line should be high. To perform read operation, initially....

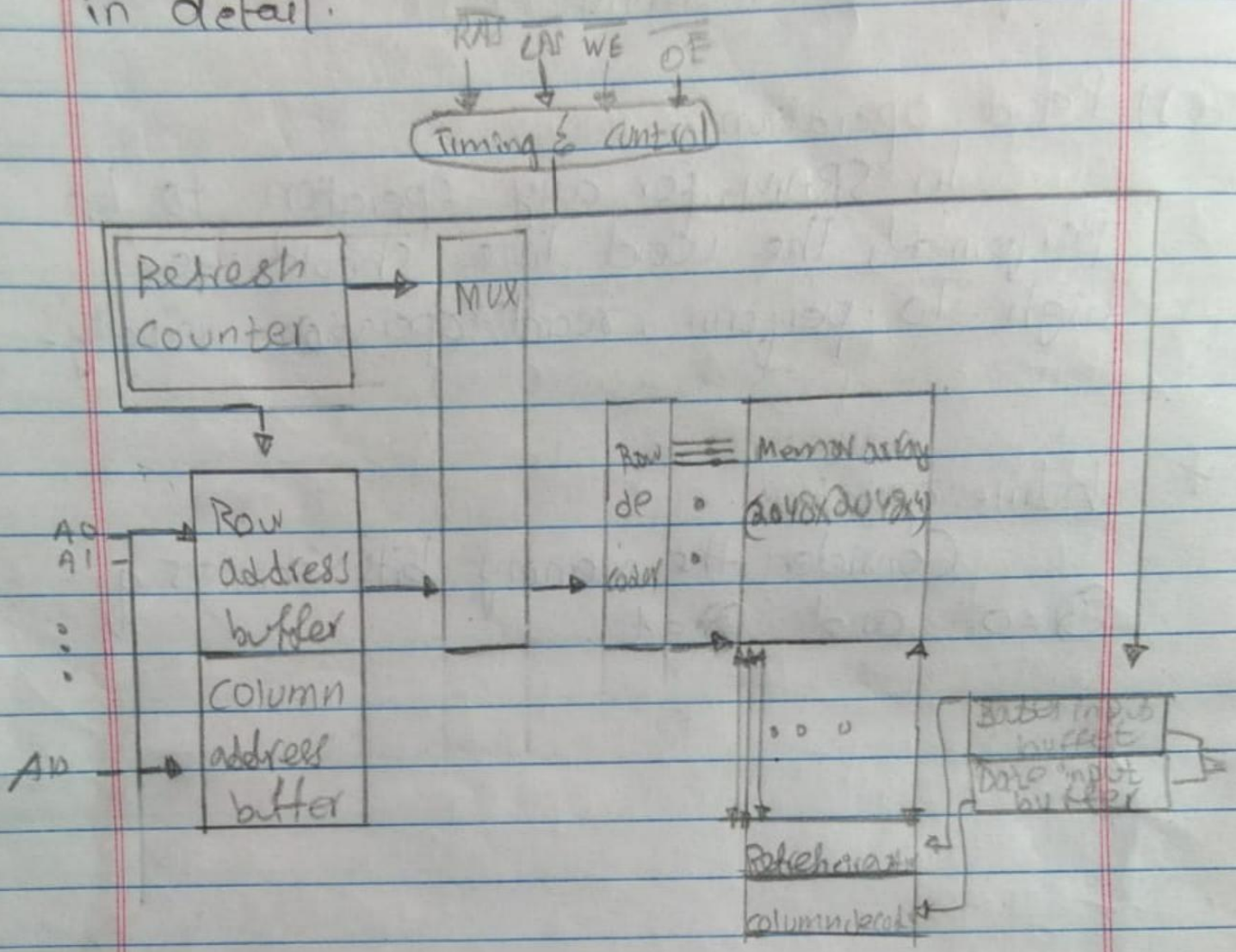
Write operation:-

Consider the memory bits consists of $Q = 0$ and $Q' = 1$.



(b) Static RAM (SRAM) cell

d) Discuss 16-Mbit DRAM (4M×4) organization in detail.



Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM chip while all data cells are refreshed.

The refresh counter steps through all of the row values. This causes each cell in row to be refreshed.

e) What are the reasons for DVD's greater capacity over CD?

Ans) The DVD's greater capacity is due to three differences from CDs:

1) Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance b/w pits along the spiral is 0.834 μm. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 μm & a minimum distance b/w pits of 0.4 μm. The result of these two improvements is about a seven-fold increase in capacity, to about 4.7 GB.

2) The DVD employees a second layer of pits & lands on top of the first layer. A dual-layer DVD has a semi-reflective layer on top of the reflective layer, and by adjusting focus, the lasers in DVD drives can read each layer separately.
The technique almost doubles the capacity of the disk, to about 8.5 GB. The lower reflectivity of the second layer limits its storage capacity so that a full doubling is not achieved.

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3) The DVD-RAM can be two sided, whereas data are recorded on only one side of a CD. This brings total capacity upto 17 GB.

Q No) Differentiate each of the following in detail.

a) EEPROM and flash memory.

EEPROM	Flash memory.
* EEPROM stands for electrically erasable Programmable read only memory	Flash memory is a non volatile memory chip used for a storage and for transferring data.
* EEPROM device can erase any byte of memory at any time.	Flash memory can only erase an entire chunk; or "sector" of memory at a time
* EEPROM user Nor type memory.	Flash memory uses NAND type memory.
* EEPROM is byte-wise erasable.	Flash is block-wise erasable.

b) Hardware failure and soft error in Semiconductor memories.

Ans A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically b/w 0 and 1. How errors can be caused by harsh environmental abuse, manufacturing defects and wear.

where as

Softerror is a random, nondestructive even that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

c) Read and write mechanisms for magnetic disk.

Ans- READ:-

The traditional read mechanism exploits the fact that a magnetic field moving relate to a coil produces an electrical current in the coil. when the surface of the disc passes under the head, it generates a current of the same polarity as the one already recorded. Such single heads are used in floppy disks systems and in order rigid disk systems. The read head consists of a partially shielded magnet resistive (MR) sensor. The MR design allows higher-frequency operation, which equation to greater storge densities & operating speeds.

Write:-

The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field. Electric pulses are sent to the write head, & the resulting magnetic

patters are recorded on the surface below, with different patterns for positive & negative currents. An electric current in the wire induces a magnetic field across the gap, which in turn magnetizes a small area of the recording medium, reversing the direction of the current reverses the direction of the magnetization on the recording medium.

d) Parallel access & Independent access RAID schemes.

Ans Parallel access RAID:-

In parallel access array, all member disks participate in the execution of every I/O request. Typically, the spindles of the individual drives are synchronized so that each disk head is the same position on each disk at any given time.

As in the other RAID schemes, data striping is used, In the case of RAID 2 & 3. the strips are very small, often as small as a single byte or word.

Independent Access RAID:-

In an independent access array, each member disk operates independently so that separate I/O requests can be satisfied in parallel. Because of this, Independent access array are more suitable for applications that require high I/O request rates and are relatively less suited for application that

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require high data transfer rates.

* As in the other RAID schemes, data striping is used In case of RAID 4 through 6, strips are relatively large.

e) HD DVD and Blu-ray DVD.

Ans) HD DVD players have been much cheaper than Blu-ray machines, but Blu-ray disc have more Storage space and more advanced protection against piracy.

* Both versions deliver Shap resolution
* Blu-Ray has 25 GB capacity (50 GB for dual-layer) and is more expensive.
* HD-DVD has 15 GB (30GB for dual layer) and is cheaper than Blu-Ray.

Q.No 3) Write note on each of the following.

a) Memory Access methods.

Ans There are four types of memory access methods.

1) Sequential Access:-

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single linked list. The access time depends on the location of the data. Applications of this sequential memory access are magnetic tapes, magnetic disk and optical memories.

2) Random access:-

In this method, any location of the memory can be accessed randomly like accessing in Array. physical locations are independent in this access method.

Applications of this random memory access are RAM & ROM.

3) Direct Access:-

In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. The access time depends on both the memory organization and characteristics of storage technology. The access is semi-random or direct.

Application of this direct memory access is magnetic hard disk, read/write header.

4) Associative Access:-

In this memory, a word is accessed rather than its address. This access method is a special type of random access method.

Application of this direct memory access is cache memory.

b) Principle of Locality:-

Ans The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

OR

An implication of locality is that we can predict with reasonable accuracy what instructions and data a program will use in the near future based on its accesses in the recent past.

C) Possible approaches to Catch coherency.

Ans. Following are the possible approaches to catch coherency include the following.

- Bus watching with write through:-
  Each cache controller monitor the address lines to detect write operation to memory by other bus masters. If another master write to a location in shared memory that also resides in the cache memory, the catch controller invalidates the cache entry. This strategy depends on the use of a write through policy by all cache controllers.

- Hardware transperency:-
  Additional hardware is used to ensure that all updates to main memory cache are reflected in all caches. Thus if one progessor modifies a word in it's cache, this update is written to main memory, in addition any matching words in other caches are similarly updated.

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- Non-Cachable memory:-
  Only a portion of main memory is shared by more than one processor, and this is designated as non-cachable. In such a system, all accesses to shared memory is never copied into the cache. The non-cachable memory can be identified using chip select logic or high address bits.

d) Practical issues peculiar to SSDs.
There are two peculiar issues to SSDs that are not faced by HDDs.

* SDD performance has a tendency to slow down as a device is used:-
* The entire block must be read from the flash memory and placed in a RAM buffer.
* Before the block can be written back to flash memory, the entire block of flash memory must be erased.
* The entire block from the buffer is now written back to the flash memory.

* flash memory becomes unusable after a certain number of write.

Techniques for prolonging life.

* front-ending the flash with a cache to delay and group write operations.
* Using wear-levelling algorithms that evenly distribute writes across block of cells.
* Bad block management techniques.
* Most flash devices estimate their own remaining life times so system can anticipate failure and take pre-emptive action.

(e) CD read and write operation.

Ans: Read:-

Information is retrieved from a CD or CD-ROM by a low powered laser housed in an optical disk player, or device unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit. Specifically if the laser beam falls on a pit, which has a somewhat rough surface, the light scatters and a low intensity is reflected back to the source. The areas between pits are called lands.

A land is a smooth surface which reflects back at higher intensity. The change b/w Pits and lands is detected

by a photo sensor and converted into a digital signal the sensor tests the surface at regular intervals. The beginning or end of a pit represents a 1. When no change in elevation occurs b/w intervals, a 0 is recorded.

Write:-

Recall that on a magnetic disk, information is recorded in concentric tracks.

With the simplest constant angular velocity (CAV) system, the number of bits per track is constant. An increase in density is achieved with multiple zoned recordings in which the surface is divided into a no of zones, with zones further from the centre containing more bits than zones closer to the centre. Although this technique increases capacity. It is still not optimal.

Q4) Solve the numericals.

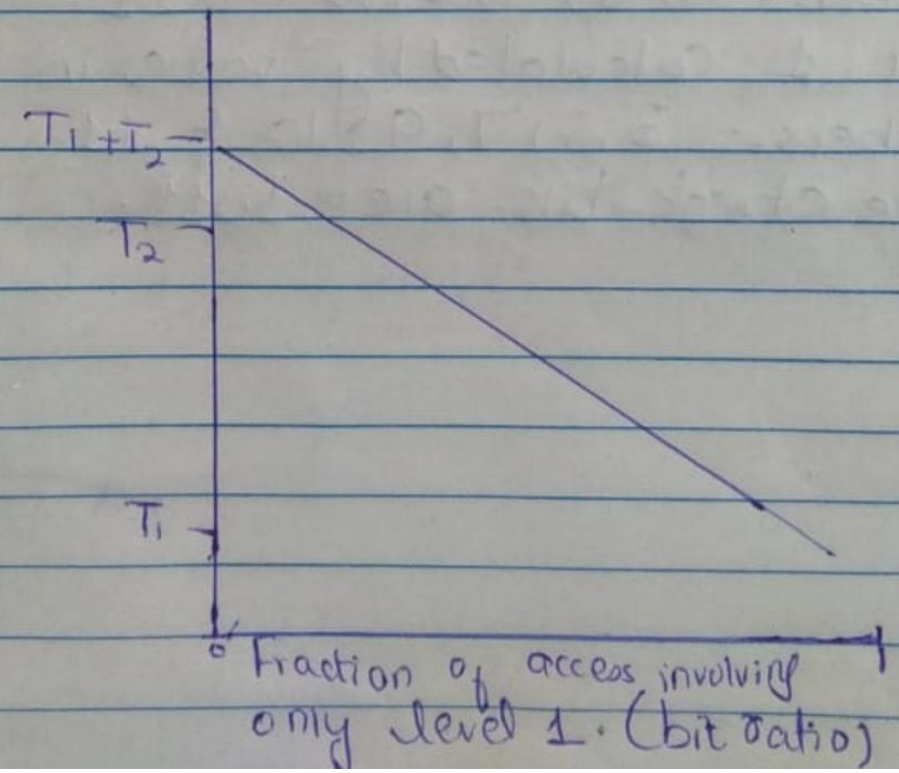
a)

In our example Suppose 95% of the memory accesses are found in Level 1. Then the average time to access a word can be expressed as

$$(0.95)(0.01\,\mu s) + (0.05)(0.01\,\mu s + 0.01\,\mu s) =$$

$$0.0005 + 0.0005 = 0.015\,\mu s.$$

The average access time is much closer to 0.01 μs than to 0.1 μs as desired.



(Part b)

Sol

Total block in the cache = 8 bytes / 16 bytes = $2^3 \times 2^{10} / 2^4 = 2^9 = 512$

No of Set = num of block in cache / 2

No of Set = 512/2

No of Set in cache = 256

No of set in Cache = 2^8

No of set = 8

Size block = 16 = 2^4

Size of memory = $2^6 \times 2^{20} = 2^{26}$

Tag = Size of memory − Size of block (set)

Tag = 26 − 8 − 4

Tag = 14

tag	Set	Size of block
14	8	4

For tag set:-

* Tag (01) / set (CB) / word (2) 177H / 0EEEH / 3H

Part (c)

Ans $M = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers 1, 2, 4 & 8.

- Check bit 8 calculated by values in bit numbers: 9, 10, 11 & 12.
- Check bit 4 calculated by values in bit numbers: 5, 6, 7 and 12.
- Check bit 2 calculated by values in Bit numbers: 3, 6, 7, 10, 10 and 11.
- Check bit 1 calculated by values in Bit numbers: 3, 5, 7, 9, 10 & 11.

Thus, the check bits are: 1011.

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Part (D)

Ans - (Solution)

7200 revolution in 60 sec

1 revolution in $\frac{60}{7200}$ OR

1 revolution in 6ms.

1 revolution = Covering one entire track = 500 sector

500 sector = 6ms

1 Sector = 8 microsecond.

Now there are 2 different things.

① 2500 Sectors so time = 2500 × 8ms = 20ms.

② 1.28MB = 1342177.28 bytes or 2621.44 Sectors = 2622 sectors = 20.976ms.

Total time case

Case ① 4 + 2 + 20 = 26ms

Case ② 4 + 2 + 20.976 = 26.976ms.