(2)

(1)

NAME : HAMEED KHAN
Department : BS (CS)
Semester : ~~1st~~ 4th
ID : 15066
Subject : Basic electronics
Submitted To : KHAlid HAMEED
Date : 25/6/2020

(Q5)

(a)

advantages of BJT :-

1. it has a large gain bandwidth.
2. it shows better performance at high frequency.
3. it has a better voltage gain
4. it has high current density.
5. it can be operated in low or high power applications.

disadvantages of BJT :-

1. The BJT is more on effect or reading
2. it has a very complex base control so it may lead to confusion

and requires a Skilful handing

(3) it is more noise produced.

(4) it has a low thermal stability.

(5) The Switching frequency of a BJT is low.

advantages of FET:-

(1) FETs have better thermal stability.

(2) FET are voltage Controlled devises.

(3) FET. are less ~~Eff~~ effect by ~~reading~~ reddiation.

(4) FETs Produced less noise.

disadvantages of FET:

(1) FETs have a poor frequency response due to its high input capacitance.

(2) FETs Can be damaged due to the static electricity.

(3) FETs have a very poor linearity and generally they are less linear than Bipolar junction Transister.

③

Q5

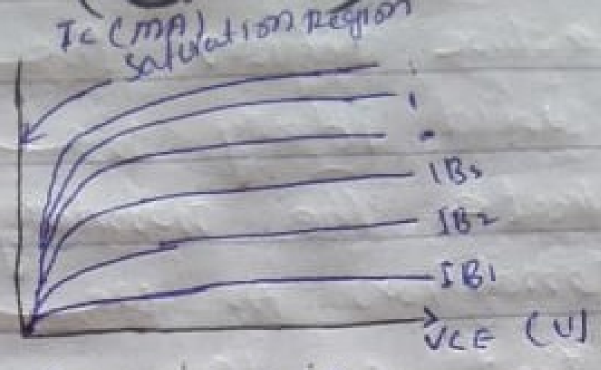
(b)

When the drain voltage is increased, the positive drain potential opposes the gate voltage bias and are reduces the surface potential in the channel. The channel inversion layer charge decreases with increasing drain-source voltage and ultimately it becomes zero when the drain source voltage equal to

$$\left(V_{GS} - V_{GS(TH)}\right)$$

This point is called the channel pinch-off voltage where the drain current becomes saturated.

(Q No 2)



IB1 < IB2 < IB3 ; ——

(*) * As the magnitude of VCE decrease there comes a point when the collector voltage becomes less than the base voltage. When this happens the transistor regain which is highly non-linear and is not usable for amplification.

(*) The cut off region of operation access for base currents near zero in the cut off region the collector current approach zero in a non linear manner and is also avoided for amplification application.

(*) The linear region is where we want to be for one

Complipaction. in the linear for active region the Course would ideally be to indicate the normally off condition As we know that for Vcis exceeding the Threshold voltage. Vcis T, on N-Type inversion layer connecting the Source to drain is created

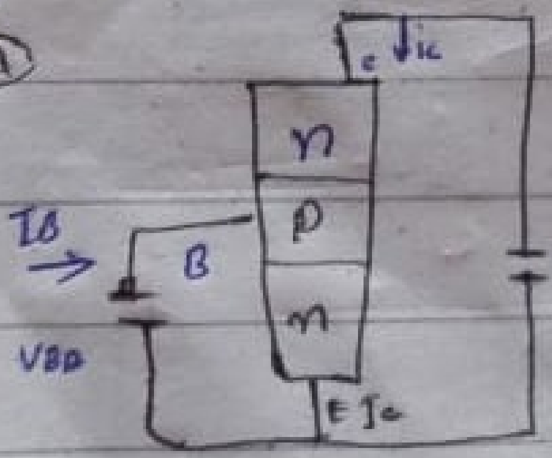
(Q3) (b)

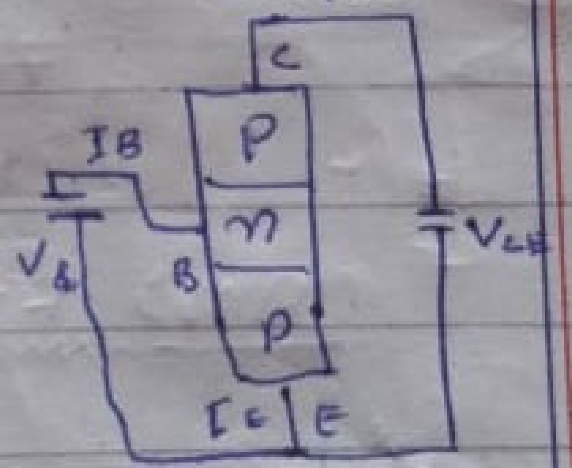
(1)

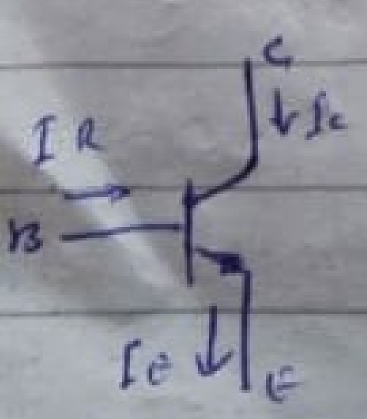
Common emitter:-

When the emitter terminal is Common to both the input and the output Circuit the mode of operation is called The common emitter or the ground emitter configuration of the transistor.

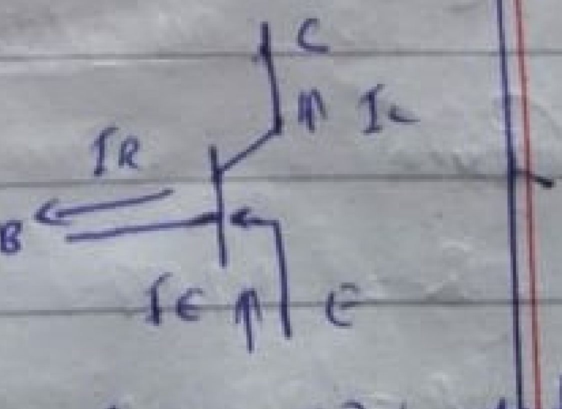
(a)







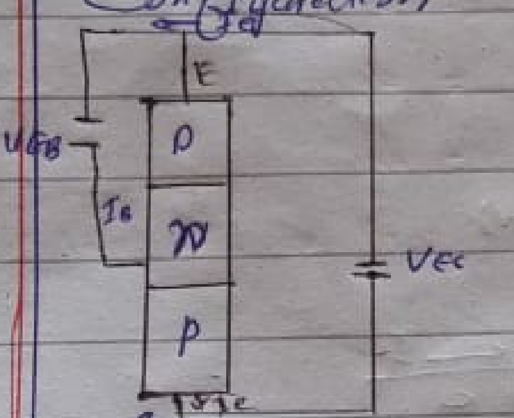
(n-p-n transistor)

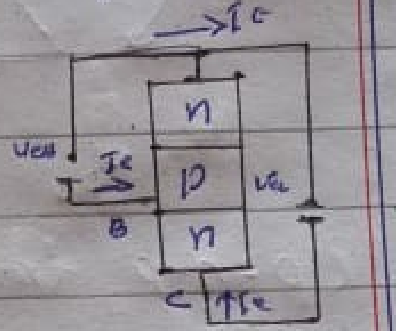


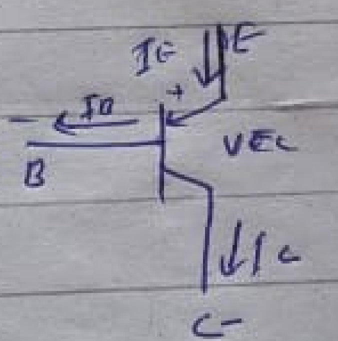
(p-n-p) transistor

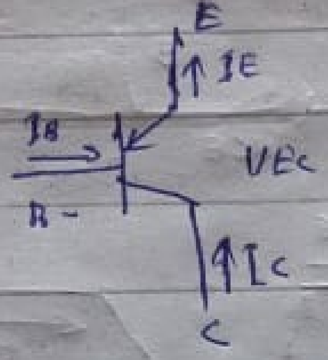
(2) Common Collector:-

When the collector terminal of the transistor is common to both the input and the out put terminals the mode of operation is known as the common collector mode or the ground collector configuration.



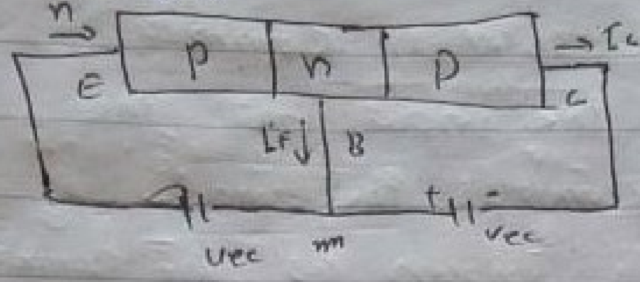


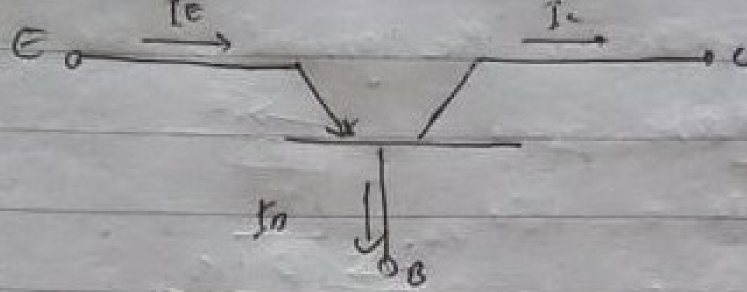




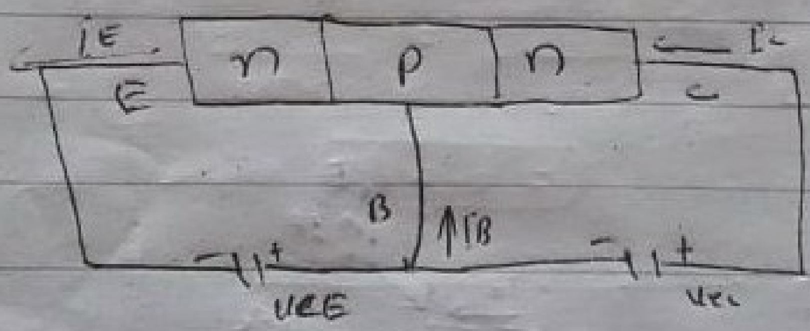
(3) Common Base:

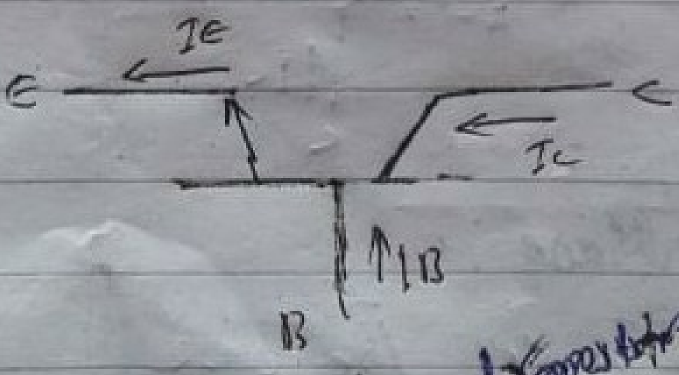
in this mode the base terminal is common to both to input and the output circuits this mode is also referred to as the grounded base configuration.





(p-n-p transistor)





n-p-n transistor

Q1 **Part (b)**

Given data:→

Load Resistance $R_L = 1500\,\Omega$

Input current $= E_i = 24$

Resistance $= R = 470\,\Omega$

Required data:→

load voltage $= V_L = ?$

sol:→ As we know that

$$V_L = \frac{R_L E_i}{R + R_L}$$

puting values

$$\Rightarrow V_L = \frac{1500 \times 24}{470 + 1500}$$

$$\Rightarrow V_L = \frac{36000}{1970}$$

$$\Rightarrow \boxed{V_L = 18.27\,V}$$

Result:→ $\boxed{V_L = 18.27\,V}$

Q1 part (a)

Given

$I_s = \frac{24v}{470\Omega}$

51.06 mA

Special purpose diode

Since the load voltage is 15

$I_2 = \frac{15v}{1.5 K\Omega}$

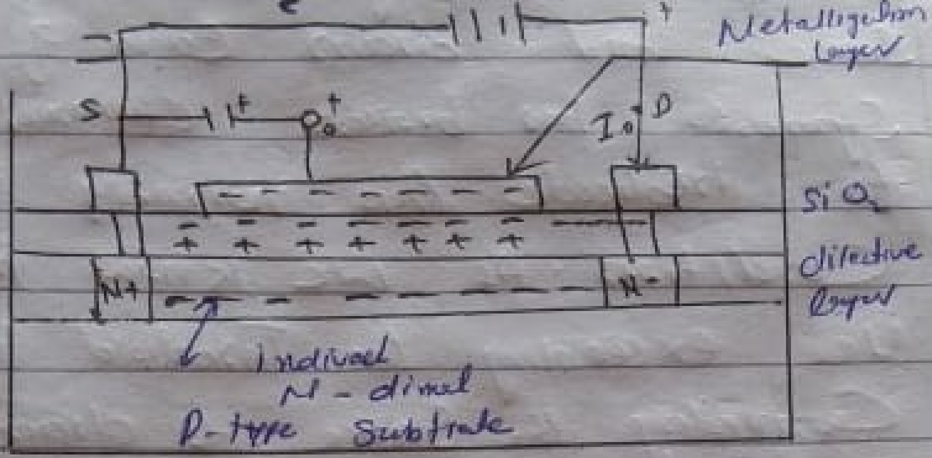
$I_2 = 10 mA$

The zener current is the diff b/w tow current

$I_z = 51.06 mA - 10 mA$

$I_z = 41.06 mA$ Ans

(Q4)



The current IDS at VGS z=0 is very Small being of the order of a few nano-compress when the VG is made possitive The drain Current ID increases slowly at first and the much more rapeidly with the drain Current ID attain Some defined Small value Say 10UA A Current ID1 ON Corresponding approximatly to the maximum value given on the drain Characteristics and the value of VGS required to give this Current Vis ON are also Uisally given on the monofecteres date

Sheet for zero value of V_{GS} the E-MOSFET So off because there is no conducting channel between Source and drain Each of Schematic Symbols has broken channel line to indicate this normally OFF Condition. As we know that for V_{GS} exceeding the Threshold layer Connecting the Source to drain is creded.

The END