Salman Khan ID # 14974 Sir-M. AMIN

Q1:- Give Answer to each of the following.

A.

Ans:- (ISU) Instruction Sequence Unit:- Determine the Sequence in which Instructions a executed in what reffer to as a super scaler architecture.

(IFU) Instruction Fetch Unit :- Logic for fetching instruction.

(IDU) Instruction decode Unit:- The IDU is fed from the IFU buffers, and is responsible for the parsing in decoding of all Z/Architecture operation Code.

(LSU) Load- Store Unit :- It is responsible for handling all types of operand accesses of lengths, modes, and formate as dufined in the Z/architecture.

(XU) (translation Unit) :- The Unit translate logical addresses from Instuctions into physical addresses and main memory it Contain TLB Used to Speed of memory access

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(FXU) Fixed point Unit :-
The FXU executes fixed point arthematic operations.

(BFU) Binary - Floating - Unit :-
The BFU handles all binary and hexa decimal floating point operations; as well as Fixed point Multiplication operations.

(DFU) Decimal Floating poin- Unit :-
The DFU handles both fixed point and floating point operation on number that are stored the decimal digits.

(RU) (Recovery Unit) :-
The RU keeps a point Copy of the Complete state of the System that includes all registers Collect hardware fault signals.

COR (dedicated Co- processor) :-
The COP is responsible for data Compression and encryption funtion for each Core.

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L1 - Cache:

This is 64KB L1 instruction Cache allowing The IFU to prefetch Instruction before they are needed.

L2 Control:

This is Control logic that manage the trafic through the two L2 Caches.

Data L2:

A 1 MB L2 data Cache for all memory traffic other then instruction.

Instruction L2:

A 1 MB L2 Instruction Cache.

B.

Ans: The IAS operate by respectively Performing as Instruction cycle each the Instruction cycle Consist of two sub-cycle.

Fetch cycle:

The opcode of next instruction is loaded into the IR and the address portion is loaded in to the MAR.

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The Instuction may be taken from the IBR or it can be obtained from memory by loading a word into MBR and then down to the IBR, IR and MAR.

Execute Cycle:

The Controlls Circuitry interprets the opcode and execute the Instruction by sending out the appropriate Control Signal Signal to Cause data to be moved or an operation to be performed by the ALU.

C.

Ans: Embedded System:-

The term embedded System reffers to the Use of electronic and Software with in a product is opposed to a generall purpuse Computer, such as liptop, or Desktop System. today many devices that Use electric power have and Embedded Computing System.

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Different embidded system Using everyday life are, cell phones, Digital Cameras, Calculators, vidio Cameras, Micro wave ovens, home Security System watching waching machine Lighting System, printer etc.

D-

Ans: Different Desktop application that require the great Power of Contemporary microprocessor based system are:

- Image processing
- Three dimensional rendering.
- Speech recognition.
- Video Conferencing
- Multimedia Authoring.
- Voice and video annotation of files.
- Simulation modelling.

E.

Ans: The tecniques Used in Contemporary processor to increas Speed are following.

- Pipelining:

Pipelining enable a Processor to work - simultinously on multiple instructions by

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Performing a different phase for each of the multiple Instruction on the same time.

- Branch prediction:

Branch prediction potentially increase the amount of work availible for the proccessor to excute.

- Super Scaler execution:

This is the ability to issue more than one instruction in every processor Clock cycle. An effect, Multi parallel piplines are used.

- Data flow analysis:

The processor analyze which instructions are dependent on each other's result. or data to creat an optimized shedule of instructions.

Speculative execution:

This enables the processor to keep its execution engines as busy as possible by executing instruction that are likely to be needed.

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F.

Ans: Discuss the problems Created due to Increase in Clock Speed and logic density of the processor are:

- Power:
  As the density of logic and the clock speed on a chip increases dissipates the heat.
- RC delay:
  The speed at which electrons can flow on a chip b/w transistor is limit by the resistance the capacitance of the metal wire Connecting them, specifically, delay increase as the RC Process Increases.
- Memory latency:
  Memory access Speed (latency) and transfer speed (throughput) lag processor Speed.

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G.

Ansr The speed of Using a parallel processor with N processor that fully exploit the parallel portion of the parogram as follows.

Speed up = Time to execute program on a single processor / Time to execute program on N parallel processor.

$$= \frac{T(1-f) + Tf}{T(1-f) + Tf/N} = \frac{1}{(1-f) + f/N}$$

H.

Ansr Mutticore s

The use of Multiple processor on the same ship provide the potentail to Increase performance with out Increasing the clock rate. Strategy is to use two simpler processors on the chip rather than one more Complex processor. with two processor larger Caches are justified.

As Caches became larger it made performance sense to Creat two and then three levels of Cache on a chip.

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MIC:

Leap in performance as well as the Challenger and developing software to exploit such a large number of Cores.

The multicore and MIC strategy involves a homogenouse Collection of a generall purpose processor on a singnal ~~MIC~~. chip.

GPUs:

Core designed to perform parallel operation the grapics data. Tradionally found on a plug-in graphics Card it is used encode the render 2D and 3D Graphics as well as procuss video used as vector processors for a variety of applications that requires repetitive Computations.

I.

Ans QPI Protocol layer:

In this layer, The packet is defined as the unit of transfer. One key fn perform in this level is Cache Coherency protocol, Which deals with making

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Sure that the memory values held in multiple Caches are Consistent. A typical data packed payload is a block of data being sent to or from a Caches.

J:
Ans:

Physical and logical Architecture of PCIe:

A root Complex device, also refferred to as a chipset or a host bridge, Connect the processor.

And a memorey subsystem to the PCI Express which fabric Comprising one or more PCIe and PCIe switch devices. PCIe link from the chipset may attach to the following kind of devices that implement.

PCIe:

Switch: The switch manage multiples PCIe streams.

PCIe end point:

An I/O device or Controller that implements PCIe such as a Gigabite ethernet switch a graphics or video Controller, disk interface, or Communications Controller.

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Legacy endpoint:
Lagacy endpoint Categor is intended for existing designs that have been migrated to PCI Express. and it allows lagacy behaviors such as used of of I/O space and locked transactions.

PCIe/PCI bridge:-
Allows older PCI devices to be Conected to PCIe- based System.

Q2: Writ short note on each of the following.

A

Ans: There are four main structural Components:

1. Central processing Unit (CPU): Controls the operation of the Computer and performs it data processing functions; often simply reffered to as processors.

2. Main Memory Stores data.

3. I/O Moves data blw the Computer and its external enviroment.

4. System interconnection: Some machanism that provides for Communication among (CPU) Main Memory. and I/O.

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B:

Ans: The Charateristics of a ~~planned~~ family are as fellows:
Similar or identical Instrution Set. In Some Cases, the lower end of family has an Instruction set that is a subset that of the top end of the family. this meanse that programs can move up but not down.
Similar or identical operation system. The same basic operating system is availible for all family members.
Increasing Speed: The rate of Instruction excution increases in going from lower to higher family members.
Increasing number of I/O ports: The number of I/O ports: The number of I/O part Increases in going from lower to higher family members.
Increasing memory size: The size of main memory increases in going from lower to higher family members.
Increasing Cost: At a given point in time the Cost of system increases in going from lower to higher family member.

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C.

Ans: A Funadamental design approach first implemented in the IAS Computer known as a Stored-program Concept. this ideas is Usually attributed to the mathematician John von Neumann.

The first publication of the Ideas was in a 1945 proposal by von Neumann for a new Computer, EDVAC (Electronic Discrete variable Computer) In 1946, Von Neumann and his Colleagues began the design of a new stored program Computer, reffered to as the IAS Computer, at the princeton Institute for advance studies.

It Consist of

A main memory which Store both data or and instruction.

An Arthemetic and logic unit (ALU) Capible of operating of binary data.

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D.

Ans:- The famouse Moores law, which was propounded by Gordon Moore; Cofounder of Intel In 1965 [moore 65] moore observed that the number of transistor that Could be put on a Singal chip was doubling every year. The pace slot to a doubling every 18 Moths in the 1970s but has sustained that rate ever since.

The Consequences of Moor's law are; propound.

1. The Cost of Computer logic and memory Circuitry has fallen at a drametic rate.
2. Because logic and memory element are placed together on more densely packed chips, the electrical path length is shortened, increasing Operating. Speed:-
3. The Computer becomes smaller, making it more Convenient to place in variety of the enviroment.
4. There is a reduction in power requirement.

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5. With more circuitry on each chip, there are fewer Interchip Connections.

E-

Ans: Instruction cycle State Diagram:
The state in instruction cycle Combe described as follows:

Instruction address Calculation (iac): Determine the address of the next instruction to be execute. Usually, this involves adding a fixed number to the address of the previous instruction.

Instruction fetch (if) :- Read instruction from its memory location into the processor.

Instruction operation decoding (iod) Analyze instruction to determine type of operation to be performed and operand (s) to be used.

Operand address Calculation (oac): If the operation involves refrence to an operand in memory or availible via I/O, then determine the address of the operand.

Operand fetch (of) :- Fetch the operand from memory or read it in form I/O.

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Data operations: (DO):
Perform the operation Indicate in the Instruction.
Operand Store (OS) :
WRite the result into memory or out to I/O.

F.
Ans:

Classes of Interrupts:

(i) Program:
It is generated by some Condition that occurs as a result of an Instruction excution, such as arithematic overflow, division by Zero, attempt to execute an illegal machine instruction. or reference outside a user's allowed memory Space.

(ii) Timer:
It is generated by a timer with in the processor This allows the operating system to perform Certain functions on a regular basic.

(iii) I/O:
It is generated by an I/O Controller, to Signal normal Completion of an operation, request

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Service from the processor, or to signal of a variety of error Condition.

IV. Hardware Failure:
It is generated by a failure or money such as power failure or memory parity error.

Q.

Ans: Bus Interconnection Scheme:
The most common Computer Interconnection structures are base of the use of One or more system buses.
A system bus Consist, typically, of from about fifty two hundered. of separate line. The line Can be classified into three ftn group; data, address, and Control lines.

a) Data lines:
The data lines provide a path for moving data among system modules. these lines collectively, are called the data bus.

b) Address lines:
The address line are use to designate the source of destination of the data on the data bus.

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The width of the address bus determine the maximum possible memory Capacity system.

(c) Control lines:-

The Controll lines are used to Controll the access to and the use of data and addres line because the data and addres lines are shared by all Components. there must by a meomse of Controlling their use typacal Control line include. Memory write, Memory read I/O write, I/O read transfer ACK. Bus request, Bus grant Interrupt request Interrupt ACK, Clock and Reset.

B.
Ansi

Q3:
A.
Ansi: Computer architecture reffers to those attributes of System visible to a programmer or, put another way, those attribute that have a direct Impact on the logical excution of instruction of program. A term that is often used interchangebly with Computer

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orchitecture is Instruction Set architecture (ISA). Computer Organization: Refferce to the operational Unit in their interconnection that realize the architectural Specipication. Example of architectural attributes include The instruction sets the number of bits used to represent various data types. e.g numbers, (characters) I/O machanisms, and tecnique for addressing memory.

B.

Ansr The Current x86 offering represent the result of decades of design effort on Complex instruction Set Computer (CISCs). The x86 incorporates the Sophisticated design principles once found only on mainframes the Supercomputer and Service ars an exellent example of CISC design in the reduce instruction. An alternative approach to processor design is the reduced Instruction set.

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Computer (RISC) :-

The ARM architecture is used in a wide variety of embedded system and is one of the most powerfull of best designed RISC - based system on the market In this section and the Next, we provide a brief overwiew of these two systems.

C.

Ans: Micro processor :-

Micro processor chip include registers, an ALU, and some sort of control unit or instruction processing logic. As transistor density increased. it become possible to increase the company of the instruction set. architecture, and Ultimatly to added memory and more than one processor.

A microControllers

It is a single chip that Contain the processor, non- volatile memory for the program (ROM), volatile memory for input and out put

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(RAM), a clock a clock and an I/O Control unit the processor portion of the microcontroller has a much lower Silicon Area than other microprocessor and much higher energy effiency.

D.

Ans:- The Cortex-A and Cortex-A50 are application processor. intendend for mobile. device such as smartphone and e book reader as well as Consumer devices such as degital tv and hoome gateways e.g DSL and cable internet modems) these processor run at higher clock frequency (over 1GHz) and support a memory management unit (MMU).

The Cortex-R is designed to support real-time applications in which the timing of events need the Controlled with rapid response to events. they Can run at a fairly high clock frequency (e.g 200MHz to 800 MHz) and have very low response lateney.

Cortex M series processor have been devoloped primarily

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for the microcontroller domain where the need for fast. highly deterministic. interrupt management is Cuple with the desire for extremly low gate count and lowest possible power Consumption.

E.

Ans: In the interrupt cycle, the processor checks to see any interrupts have occurred indicate by the presence of the Interrupt signal if no Interrupt are pending. The processor proceeds to the fetch cycle and fetches the next instruction of current program.

F.

Ans: A disable interrupt simply means that the prosessor Com and will ignore that interrupt request signal. If an Interrupts occurs during this time its genrally remain pending and will be checked by the processor after the processor has enabled Interrupts.

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A nested interrupt is to allows an interrupt of higher priority to cause a lower priority interrupt handler to be itself intrupted. A user programe being at t = 0 At t = 10, a printer interrupt occurs, user information is placed on the system stack and excution continouse at the printer Inturrupt service routine (ISR) while this routine is still executing at t = 15 a communication Interrupt occurse.

Q.

Ans: Programming in Hardware:-
The "program" is an form of hard ware and is termed a hard wired program.
Suppose we constract a general purpose configuration of arithematic and logic person of ftns. This set of hardware will peform various ftn on data depending on control signals applied of the hard ware, the system accept data and produces result.

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Programming in Software:-
The new method of programming which is a sequence of codes or instruction is called software programming.

In this method, programing is much easier Instead of rewiring the hardware of each new program. all we need to do is provide a new sequence of codes. Each codes and in effect an instruction any part of the hardware interept each Instruction, and part of the hard ware interepts each Instruction and genrated Controll signals.

Q4:
Ans:

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Q4: Solve each of the following.

A.

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB

a)

Ans: Here is simple way to Undrestand this problem. Contents are divided up into two 5 bit Instruction, LH and RH

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since this is hexadeeimal from you have to Convert the number to binary form:

(Use the IAS Instruction set)

LH instruction

01 = 00000001 = LOAD M(X)

M(X) refers to the memory address location 0FA

The first 5 bite of 08B should read - Load M (0FA)

RH instruction;

21 = 00100001 = STOR M(X)

M(X) reffers of the money address location 0FB

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The second 5 bits of 08A should read - STOR M(0FB)
Finally the assembley language Code for 08A 010FA210FB is
LOAD M (0FA)
STOR M (0FB)

2. Here is a simple way to understand this problem:
Content are divid are two 5 bit instruction, LH and RH.

LH instructor = 010 FA
opCode = 01
address = 0FA
RH instruction = 0F08D
opCode = 0F
address = 08D.

Since this is an hexadecimale from you have to Convert the number to binary form
(Use the IAS instruction set)
LH instructions
01 = 00000001 = LoaD M(X)
M(X) reffers to the memorey address location 0FA.
The first 5 bit of 08B should read - LOAD M(0FA)
RH instruction
0F = 00001111 = jump+M(X 0:19)
reffers to the memory address

3.

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Location 08D
The second 5 bits of 08B should read - jump + M (08D, 0:19)
Finally the assembly language Code for 08B 010FA0F08D is

LoaD M (0FA)
Jump + M (08D, 0:19)

3. Here is simple way to understand this problem:
Content are divide up into two 5 bit instructions, LH and RH
LH instraction, LH and RH LH
Instruction = 020FA
opcode = 02
address = 0FA
RH Instruction = 210FB
opcode = 21
address = 0FB
Since this is in hexadecimal from you have to Convert the number to binary form.
(Use the IAS Instruction Set)
LH instruction;
02 = 00000010 = Load - M(X)
M(X) reffers to the memory address location 0FA
The first 5 bits of 08C should red - Load - M(0FA)
RH instructions

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21 = 00100001 = Story M(X)
M(X) reffers to the memory address location OFB.
The second 5 bite of 08C should read - STOR M (OFB)
Finally the assembly language Code for 08C 020FA210FB is.
LOAD - M (OFA)
STORM (OFB)

1

b- b-

Ans- 1. In 08A address, the M(OFA) transfer to the accumulator and transfer Content of accumulator to memory location OFB.
2- In 08B address, the M(OFA) transfer to the accumulator and take next instruction from left half of M (08D)
3- In 08C address, the - M(OFA) transfer to the accumulator and transfer Contents of accumulator and transfer Contents of accumulator to memory location OFB.

Sabaan Iqbal ID # 14974

C.

Ans

Effective cpi:

$CpI = (1*46000) + (2*33000) + (4*29000)/100$

$CPI = 162000/100$

$CPI = 1620$

MIPS Rate:

MIPS Rate = 60 MHz / 1620 * 106

Mips Rate = 60 * 106 / 1620 * 106

Mips rate = 60 / 1620

Mips rate = 0.037

Execution Time:

$T = Ic\ (Mips * 106)$

$T = 104000 / 0.037 * 106$

$T = 104000 / 37 * 103$

$T = 2811 * 10-3$

$T = 2.811$ Sec

D.

Ans

a. Since we have the same Instruction mix, that meanse the additional Instructions of each task Could be allocated appropriately b/w the instruction type. Therefore, the following table be gotten;

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Instruction type	CPI	Instruction Mix
Arithematic and logic	1	60%
Load/store with Cache hit	2	18%
Branch	4	12%
Memory reffrence with Caches miss	12	10%

The average cpi = (1×0.6)+(2×0.18) +(4×0.12)+(12×0.1) = 2.64.
therefore, The CPI has been Increased since the time for memory axis also is Increased.

b. Mips = 400/2.64 = 152. There is a Corresponding drop in the Mips rate.

c. The speedup factor equals the ratio of the execution times. The execution time is Calculated as the following: T = Ic (MIPS* 106)

For the one processor, T1 = (2* 106) /(178* 106) = 11 ms

For the 8 processor, each processor execute 1/8 of the 2 million Instruction plus the 25000

T8 = 2* 106 ÷ 8+0.025* 106/152* 106

T8 = 1.8 ms.

Salman Aslam IDH1149746

Therefore we have:
Speed up = Time to execute program on a single processor / Time to execute program on N parallel processor.

Speed up = 11 / 1.8

Speed up = 6.11.

d-

By depending on the information given, it is not obvious how to quantify this effect in By Amdahl's equation, therefore, it is a supposed that the fraction of Code, which is parallellizable is f = 1, then Amdahl's law decreases to Speed up = N = 8 therefore the actual speed up is only about 75% of the theoritical speed up.

E-

Ans:

a- The pc Contains 300 the address of of the Instruction. this value is loaded into the MAR.

b- The value in location 300 which is the Instruction with the value 1940 and hexadecimal is loaded into MBR

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and the pc is incremented. these two step can be done in paralled.

c. The value in the MBR is loaded into the IR.

2. a. The address portion of the IR (940) is loaded into MAR.

b. The value in location 301 (which is the instruction with the value (940) is located into the MBR.

c. The value in the MBR loaded into the AC.

3. a. The value in the pc (301) is loaded in to MAR.

b. The value in location (301) (which is the instruction with the vale 5941) is loaded in to the MBR in the pc is incremented.

c. The value in the MBR is loaded into the IR.

4. a- The address portion of IR (941) is loaded into the MAR.

b- The value is location 941 is loaded into the MBR.

c. The old value of the AC and value of location MBR and the result stored AC.

5- a- The value in the pc 302 is loaded into the MAR b the value in the location 302 (which is the instruction with the value 2941)

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is loaded into the MBR, and the pc is Incremented. e.
c. The value of MAR is loaded into the IR.

6. a- The address portain of the IR (941) is loaded into the MAR.
b- The value and the AC is loaded into the c. MBR is stored in location 941.

F

Ansa a- $224 = 16$ MBytes
b- (1) if the local address bus in 32 bits. the whole address Cambe transfered it one decoded in memory. However, because the data bus is only 16 bits it will requires 2 cycle to fetch a 32 bit instruction or operand.
(2) The 16 bits of the address placed on the address bus. Can't access the whole memory. thus a more Complex memory interface Controll is needed to latch the first part of the address and then the second part.
(3) a- This value in the pc 301 is loaded in program.
c- The program Counter must be at least 24 bits typically a 32-bit micro processor with

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have a 32 bit external address bus and a 32 bit program Counter, Unless Onchip segement register are used that may work with a smaller program Counter. if the instruction register to Contain the whole Instruction. it will have to be 32 bit long; if it will Contain only the opcode (Called the opcode register) then it have will be 8 bits long.

Q6

Ans: A ~~byte~~ bus cycle takes 0.25 μs, so a memory cycle takes 1 μs if both operand are even aligned! it takes 2 μs to fetch the two operands if one is odd aligned, the time required is 3 μs. if both are odd aligned the time required is 4 μs.