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Q= what are the four main functions of a computer?

Data processing:-

Data may take a wide variety of forms & the degree range of processing requirements is broad.

Data Storage:-

The computer perform a long term data storage function. file of data are store on the computer of subsequent retrival & update.

Data movement:-

When data are moved over longer distances, to or form a remote device the process is known as "data communication"

Control:-

within the computer, a control unit manages the computer's resources & orchestrates the performance of its functional parts in response to instructions.

B: Figure 01 shows the IBM zEnterprise EC12 core layout Briefly explain the function of each area.

ISU (Instruction Sequence unit):-

Determines the sequences in which instruction are executed in what is reffered to as a Superscalar ~~arthi~~ architecture.

IFU (Instruction fetch unit):-

logic for fetching instruction.

IDU (Instruction decode unit):-

The IDU is fed from the IFU buffers, & is responsible for the parsing & decoding of all z/architecture operation code.

LSU (load-store unit):-

its responsible for handling all types of operand accesses of all lengths, modes, & formats as defined in the z/architecture.

XU (translation unit):-

This unit translate logical addresses from instruction into physical addresses in main memory. it contain TLB used to speed up memory access.

FXU(fixed point unit):-

The FXU executes fixed-points arithematic operations

BFU(binary floating unit):-

The BFU handles all binary & hexadecimal floating operations, as well as fixed point multiplication operations.

DFU(decimal floating point unit):-

The dfu handles both fixed point & floating point operation on numbers that are stored as decimal digits.

RU(Recovery unit):-

The RU Keep a copy of the complete state of the system that includes all registers collects hardware fault signal.

COP(dedicated co-processor):-

The cop is responsible for data compression & encryption function for each core.

1- Cache:-

This is a 64-KB L1 instruction code cache allowing the ifu to prefetch instructions before they are needed.

L2 control:-

This is the control logic that manages the traffic through the two L2 cache.

Data L2:-

A -1 MB L2 data cache for all memory traffic other than instructions.

insty-L2:-

A1-MB L2 instruction cache.

C:- Discuss the IAS operation using the flowchart in Fig02.

Ans:- The IAS operates by respectively performing as instruction cycle. Each instruction consist of two sub-cycle.

Fetch cycle:-

The opcode of next instruction is loaded into the ~~MAR~~. IR. & the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, & then down to the IBR IR & MAR.

Execute cycle:-

The control circuitry interprets the opcode & execute the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by ALU.

D:- For each of the following example, determine whether this is an embeded system explaining why or why not.

a. Are programs that understand physics &/or hardware embeded? eg one that uses finite-element methods to predict fluid flow over airplane wings?

Ans:- NO, these programs are never considred to be embeded because they ~~at~~ are not an integral component of a larger system.

b:- is the internal microprocessor controling a disk drive an example of an embeded system.

Ans:- yes, regardless of what the disk drive is used for. The software (firmware, actually) with in the disk drive

control the HDA(head disk assembly) hardware & is hard real time as well.

C:- I/O drivers control hardware, so does the presence of an I/O driver imply that the computer executing the driver is embeded?

ANS:- NO I/O drivers do not represent the embeded system.

d:- is the microprocessor controling the Cell phone an embeded system?

ANS:- Yes the firmware in the cell phone is controling the radio hardware.

e:- Are the computer in a big phased array radar considered embeded? These radars are 10 story buildings with one to three 100-foot diameter radiating patches on the sloped sides of the building.

ANS: Yes these computers were generally Some of the most powerful computers available when the system was built, are located in large computer

Room occupying almost one whole floor of a building & may be hundreds of meter away from the radar hardware. However the software running in these computer control the radar hardware therefor the computer an integral component of a large system.

f:- is a PDA an embeded system?

ANS:- yes PDA is an embeded system because its just like a personal computer in hand.

g:- is a traditional flight mangment system(FMS) built into an airplane cockpit considred embeded?

ANS:- if the FMS is not connected to the avionics & is used only for logistics computerization, a function readily performed on a laptop, then the FMS is clearly not embeded.

h:- Are the computer in a hardware in the loop (HIL) simulator embeded?

ANS: yes, both in the simulator & in the thing being tested in the HIL simulator Hardware is being

controlled on both sides.

i:- is the computer controling fuel injection in an automobile engine embeded?

Ans:- Yes its a part of a large system, the engine & its directly monitoring & controling the engine thsough special hardware

j:- is the computer controling a pacemaker in a person's chest an embeded computer?

ANS:- Yes in this case of "the" system is the combination of the pacemaker & the person's heart.

Q. write a note on each of the following?

A:- Main Structural components of a computer:-

There are four main structual components:-

Similalar identical instruction set:-

* CPU:-

control the operation of the computer & performs it data processing functions, often simply

Referred to as processor

* Main memory:-
  Stores data

* I/O:- Moves the data between the computer & its the external movement.

* System interconnection:-
  Some mechanism that provides for communication among cpu, main memory, & I/O.

B:- Key characteristic of a planned Computer family.

The characteristic of a family are as follows.

* Similalar or identical instruction set:-
  In some cases the lower end of the family has an instruction set that is a subset of that of the top end of the family. This mean that program can move up but not down.

* Similar or identical operating system:-
  The same basic operating system is available for all family members.

* increasing Speed:-
The rate of instruction execution increases in going from lower to higher family members.

* increasing numbers I/O ports:-
The number of I/O ports increases in going from lower to higher family members.

* Increasing memory size:-
The size of main memory increases in going from lower to higher family members.

* increasing cost:-
At a given point in a time the cost of a system increases in going from lower to higher family members.

C:- Stored program counter:-

ANS:- A fundamental design approach first implemented in the IAS computer is known as the stored program concept. This idea is usually attributed to the mathematician john von neumann.

* The first publication of the idea was in 1945 proposal by von Neumann for a new computer

the EDVAC (Electronic discrete variable computer).

* in 1946, von neumann & his collagues began the design of a new stored-program computer, keffered to as the IAS computer, at the princeton institute for advance Studies.

it consist of

* A main memory which stores both data & instructions.
* An asthimatic & logic unit (ALU) capable of operating on binary data.

D:- MOORE'S Law:-

The famous moore's law which was propounded by gordon moore cofounder of intel in 1965 (MOOR65). Moore observed that the number of transistors that could be put on a single chip was doubling every year. The place slowed to a doubling every 18 months in the 1970s but has sustained that rate ever since

The consequence of moore's law are profound:

1:- The cost of computer logic & memory circuitry has fallen at a dramatic rate.

2:- Because logic & memory elements are placed closer togther or more densely pack chips, the electric path length is shortned increasing operating Speed.

3:- The computer become smaller, making it more convenient to place in a variety of enviroments.

4:- There is a Reduction in power Requirements.

5:- with more circuitary on each chip there are fewer interchip connections.

Differentiate each of the following:-

A:- Computer Organization & Computer Architecture:-

* Computer organization:-

Refers to those attributes of a System visible to a programer or put another way, those attributes that have a direct impact on the logical execution of a program. A term that is often used interchanbly with computer architecture is instruction set architecture (ISA)

* Computer architecture:-

Refers to the operational unit & their interconnection that Realize

the architectual specification
example of architectual attributes
include the instruction set
the number of bits used to
represent various data types (e.g numbers,
character) I/O mechanism & techniques
for addressing memory.

* RISC & CISC

The current x86 offerings represent
the result of decades of design effort
on complex instruction set computers
(CISC). The x86 incorporates the
sophisticated design principal
once found only on mainframes &
Supercomputers & serves as an execellent
example of CISC design

* An alternatives approch to processor
design is reduced instruction set
computer (RISC) The ARM architecture
is used in a ~~ARM~~ wide variety of embeded
system & is one of the most powerful
& best designed RISC based system
on the market. in this section
& the next, we provide a brief
overview of these two systems.

C:- Microprocessor & Microcontroller :-

* Microprocessor:-

Chips include registers an ALU & some sort of control unit or instruction processing logic. A transistors density increased it became possible to increased it ultimately to add memory & more than one processor

Microcontroller:-

is a single chip that contains the processor, non volatile memory for the program (ROM) volatile memory for input & output (RAM) a clock & an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microproccessor & much higher energy effecieney.

D:- Cortex-A, Cortex-B, & Cortex-M

The cortex A & cortex-A50 are application processor intended for mobile devices such as Smartphones & eBook readers, as well as consumer devices such as digital tv & home gateways (e.g DSL & cable internet modems) These processor run at higher clock frequency (over 1 GHz) & support a memory

managment unit (MMU)

* The cortex-R is designed to support real time applications, in which the timing of events need to be controlled with rapid response to events. They can run at a fairly high clock frequency (e.g 200MHz to 800MHz) & have very low response latency.

* CORtex-M Series processor have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt mangement is coupled with the desire for extremely low gate count & lowest possible power consumption.

Qu Solve each of the following:

A:- Given the memory contents of the IAS computer shown below,

Address contents

1:- 08A010FA210FB

2:- 08B010FA0F08D

3:- 08C020FA210FB

A:- Show the assembly language code for the program, starting at address 08A.

ANS:- Here is a simple way to understand this problem:

Contents are divided up into two 5 bit instruction LH & RH

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since this is hexadecimal form you have to convert the number to binary form: (Use the IAS instruction set)

LH instruction:

01 = 00000001 = Load M(x)

M(x) refer to the memory address location 0FA

The first 5 Bits of 08A should read - load M(0FA)

RH instruction:-

21 = 00100001 = STOR M(x)

M(x) refer to the memory address location 0FB

The second 5 BITS of 08A should read - STOR M(0FB)

Finally the assembly language code for 08A 010FA210FB is

LOAD M(OFA)
STOR M(OFB)

2:- Here is a simply way to understand this problm:

Contents are divided up into two 5Bits instruction LH & RH.

LH instruction = 01 OFA

opcode = 01

address = OFA

RH instruction = OF0 8D

opCode = OF

address = 08D

Since this IS in hexadecimal from you have to convert the number to binary form: (Use the IAS instruction set)

LH instruction:

01 = 00000001 = Load M(x)

M(x) refers to the memory address location 08D

The first 5 bits of 08B should read -

jump + M(08D, 0:19)

Finally the assembly language for 08B 0101FA01F08D i's

Load M (OFA)

jump + M(08D, 0:19)

3:- Here is a simple way to understand this problem

Contents are divided up into 5 bits instruction LH & RH

LH instruction = 020 FA

opcode = 02

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since this is in hexadecimal from you have to convert the numbers to binary form :-

(Use the IAS instruction set)

LH instruction:

02 = 00000010 = Load - M(x)

M(x) refers to the memory address location 0FA

The first 5 Bits of 08C should read - load - M(0FA)

RH instruction:

21 = 00100001 = STOR M(x)

M(x) refers to the memory address location 0FB

The second 5 Bits of 08C should read - STOR M(0FB)

Finally the assembly language code for 08C 020FA21 0FB is

```
load  - M (0FA)
  STOR  M(0FB)
```

B:- Explain this program ~~what~~ does.

1 In 08A address the M(0FA) transfer to the accumulator & transfer Contenents of accumulator to memory location 0FB.

2 In 08B address the M(0FA) transfer to the accumulator & take next instruction from left half of M(08D)

3 In 08C address the - M(0FA) transfer to the accumulator & transfer contenents of accumulator to memory location 0FB.