• COMPUTER ARCH •

• FINAL TERM •

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• Q NO 1 •

→ ANSWER :

(a)

→ WORD :

→ It is the unit of memory organization. The word size is dependant on number of bits used to represent an integer. : 8, 16, 32 and 64 bits.

→ Word is also called the natural unit of organization of memory.

→ ADDRESSABLE UNITS :

→ These are the smallest locations which can be uniquely addressed.

→ The addressable units are word internally.

→ These are clusters on M$ Disk.

→ UNIT OF TRANSFER :

→ It is the maximum number of bits that

(2)

can be written or read into the memory at a time.

→ In case of main memory, it is mostly equal to word size.

→ In case of external memory unit of transfer is not limited to word z size. It is larger and called blocks.

③ (b)

→ LRU AND LFU REPLACEMENT ALGO :

→ The most effective is the least recently used
LRU: replace that block in the set that has been in the cache longest. with no reference to it for two-way set adcociated, it is easily implemented.
→ Each line includes a used bit. when a line is referenced its USED bit is set to 1 and USE bit of other line in that set is set to 0.
→ When a block is to be read into the set, the line whose USE bit is 0 is used. because more recently used locations are more likely to be referenced.
→ LRU is also easy to implement for a fully associative cache. The cache mechanism keeps a seperate list of indexes to all the lines in the cache.
→ When a line is referenced it moves to front of the list, for replacement the line at the back is used.

→ **LFU :** Another posibility is least frequently used (LFU) : replace that block in set that has experienced fewer references.
→ LFU could be implemented by associating a counter with each line.

(4) (C)

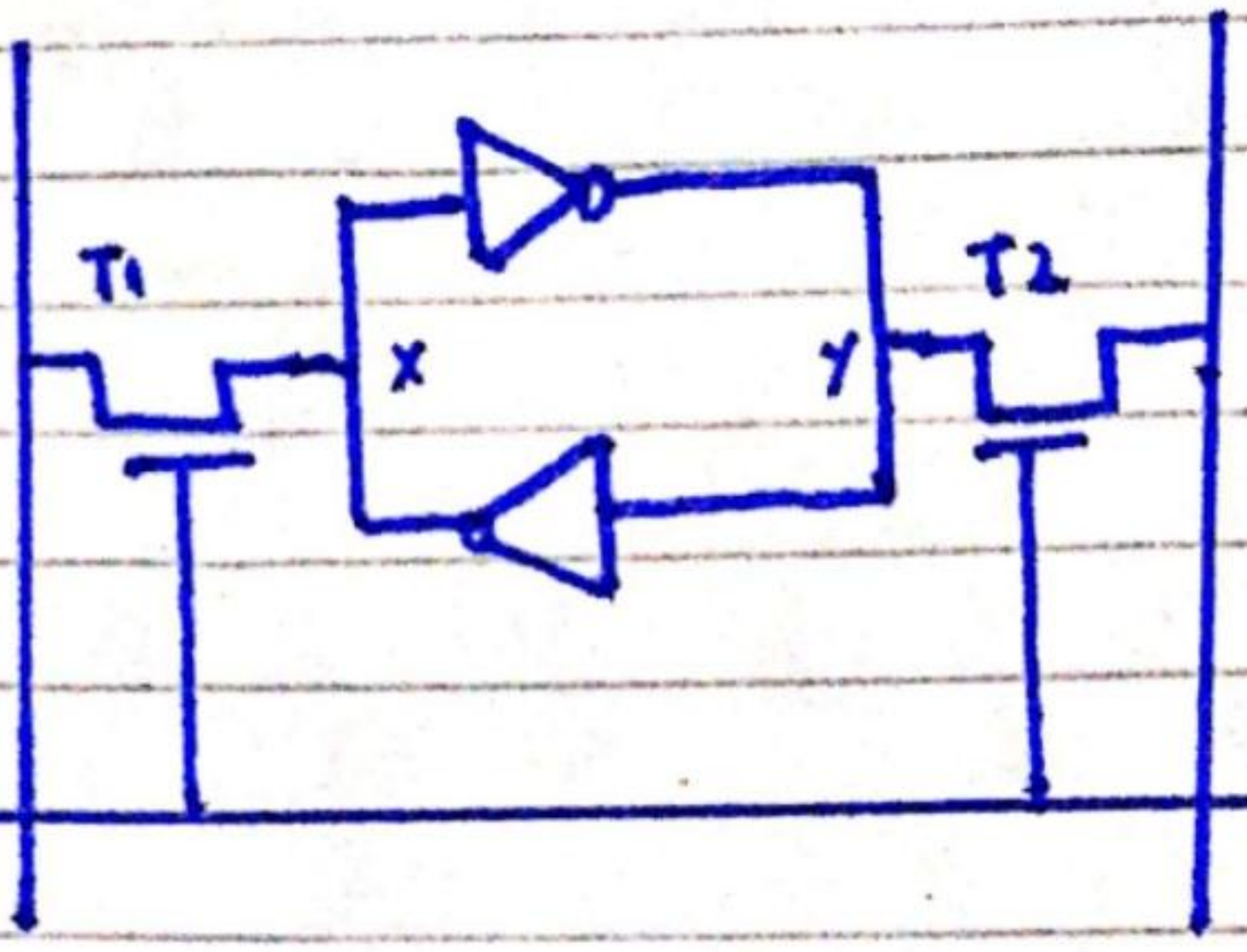
→ READ AND WRITE OPERATION'S SRAM :

→

SRAM cell is made up of two inverters cross connected to form a latch. The latch is connected to 2 bit line by transistors T_1 and T_2.

→ During read operation word line is activated to close switches T_1 and T_2. If cell is in state 1, the signal on b line is high and low on b' and vise versa if cell is in state 0.

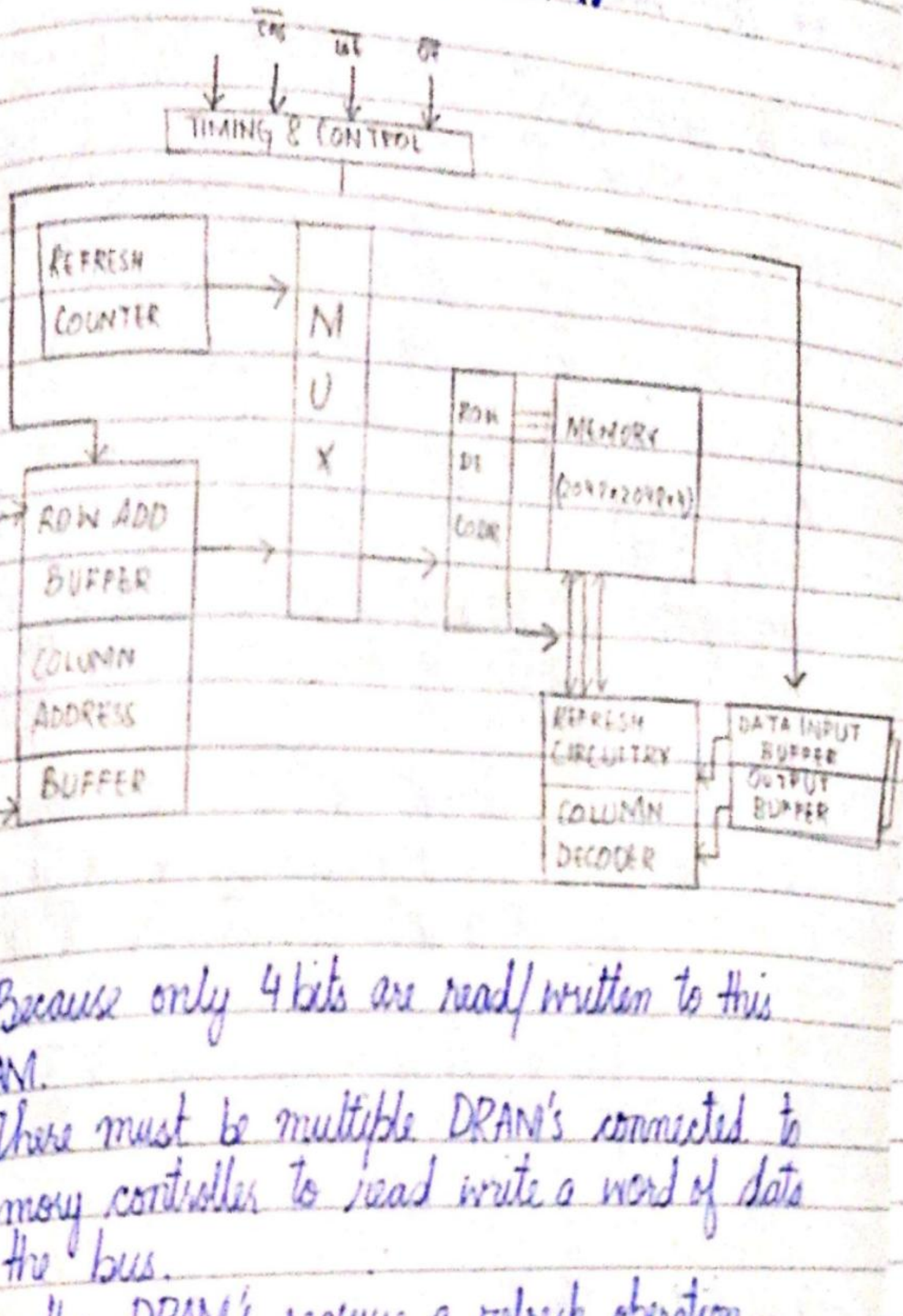
→ The Write operation, the sense / write circuit drives bit lines b and b', instead of sensing their state. It places the appropriate value on bit line b and its compliment on b' and active the word line. This forces the cell into the state, which the cell retains when word line deactivates.



⑤ (d)

→ 16-MBIT DRAM (4M x 4):

→



→ Because only 4 bits are read/written to this DRAM.

→ There must be multiple DRAM's connected to memory controller to read/write a word of data to the bus.

→ All the DRAM's require a refresh operation. A simple technique for refreshing is, to effect to disable the DRAM.

(d)

→ A technique not based on usage is to pick a line at random from among the lines.

(e)

→ DVD's GREATER CAPACITY OVER CD :

→ The greater capacity of DVD over CD is due to 3 main reasons.

→ The bits are packed more closely onto DVD.

→ The DVD uses laser with short wavelength and achieves loop spacing of 0.74 μm which is of 1.6 μm on CD which results in increase of about 4.7 GB's of capacity.

→ A DVD has a second layer of pits and lands on top of 1st layer. The laser in DVD can read each layer seperately which increases capacity upto 8.5 GB's.

(2) · Q NO 2 ·

→ DIFFERENTIATE :

(a)

→ FLASH MEMORY AND EEPROM :

→ Flash memory is a type of EEPROM, but can also be used as stand alone memory storage device, such as USB.
→ Flash is used mainly to refer to storage media and can range from a GB to hundreds of GB's.
→ On the other hand EEPROM is mostly reserved for permanant code storage in ic-chips. ranging from kilobytes to a couple of MB's.
→ flash memory incorporates the use of floating gate transistors to store data.
→ EEPROM is a data memory device that uses electronic device to erase or write digital data.

→ 1. Flash is just another type of EEPROM.
2. Flash uses nand type memory while EEPROM uses NOR type.
3. Flash is blockwise erasable, while EEPROM is byte wise erasable.
4. Flash is constantly written & EEPROM is seldom rewritten.

(8) (b)

→ HARD FAILURE AND SOFT ERRORS :

→ HARD FAILURE :

→ A hard failure is caused by real error in the circuit, maybe a design bug or process defect.

→ A hard failure is related to real circuit error.

→ A hard failure is a permanent physical defect such that the memory cells cannot reliably save data.

→ Hard failures can manifest as a memory module that does not register on start and prevent booting Thus producing intermittent data corruption.

→ SOFT ERRORS :

→ In a soft error data is corrupted without any circuit error.

→ A soft error is caused by a physical error particle passing through the device i.e (alpha, neutron).

→ Soft failure is a random error that alters the contents of one or more memory cells without damaging the memory.

→ Its mainly caused by power supply issues, etc.

→ **ABSTRACT :** Memo check detects both hard & soft errors, The application response to these error types differ because hard failures are caused by

circuit itself while soft errors are caused by some external particles that destroy the data.

(C)

→ READ MECHANISM FOR MAG DISK:

→ When the disk surface passes under the read head, an electrical current of the same polarity as what is recorded is generated in the head.

→ Another method involves a partially shielded magnetoresistive sensor. This material has an electrical resistance that depends on the direction of the magnetization of the medium moving under. These changes are detected as voltage signals.

→ WRITE MECH FOR MAG DISK:

→ Electrical pulses are sent to the write head of the drive. with the resulting magnetic patterns on the surface below. The patterns are different for positive and negative currents.

→ The write head is made of easily magnetizable material.

→ A magnetic field is induced when the electrical pulses are sent to the right head.

(10)

(d)

→ PARALLEL AND INDEPENDANT ACCESS RAID SCHEMES :

→ PARALLEL ACCESS :

→ RAID levels 2 and 3 make use of a parallel access technique.

→ In a parallel access array RAID scheme all member disk participate in the execution of every I/O request

→ Typically the spindles of the individual drive are synchronized so, each disk head is in the same position on each disk at any given time.

→ INDEPENDENT ACCESS :

→ RAID level 4 utilizes independant access technique.

→ Each member disk operates independantly unlike RAID 2 and 3

→ In independant access each member disk operates independantly, so that seperate I/O requests can be satisfied in parallel.

(e)

→ HD DVD AND BLURAY DVD :

→ Blu-Ray and DVD are the types of optical memo, where blu-ray provides larger space for storing HD videos while DVD offers less space.

→ Blu-Ray is high definition optical disk.

→ The name is generated by merging optical 'ray' and because it uses blue violet laser instead of red laser.

→ DVD (Digital Versatile Disk) is a technology generating a digitized compressed representation of video information.

→ KEY DIFFERENCES :

1. The blu-ray optical disk performs better than DVD in terms of storing data
2. In DVD red laser is used to fetch data whose wavelength is 650 nm while blu-ray uses blue laser in which wavelength is 405 nm.
3. A DVD can store a maximum of 7.4 GB in double layers while a blu-ray stores 50 GB in dual layers.
4. Blu-ray has higher data rate upto 36 Mbps whereas DVD's rate of transfer is 11.08 Mbps.

Q NO 3.

(a)

→ MEMO ACCESS METHODS :

→ Sequential access : sequential access is accessing data in a specific linear sequence.
eg :- Tape storage.

→ Direct Access : Direct address has data address being based on a physical location.

→ RANDOM : With random access any location can be selected at random and addressable locations in memory have unique physically wired-in addressing mechanism.

(b)

→ PRINCIPLE OF LOCALITY :

→ " Data in the vicinity of a referenced word are likely to be referenced in the near future "

(C)

→ POSSIBLE APPROACHES TO CACHE COHERENCY :

→ following are some possible approaches to cache coherency :-

→ Hardware transperency are used to see if all updates to main memory via cache are reflected in all cache.

→ Thus if one processor modifies a word in its cache, this update is thus written to the main memory.

→ Non cache-able memory : A small portion of main memory is shared by more processors and its non cacheable.

→ It can be identified using chip select logic or high address bit.

(d)

→ ISSUES PECULIAR TO SSD :

→ There are 2 issues that are peculiar to SSD and not present in HDD :

→ SSD performance has a tendency to slow down as the device is used.
→ Flash memory becomes unusable after a cutain number of writes.

(e)

→ CD R/W OPERATIONS :

→ The read and write (R/W) is a file attribute or permission that can be given to files and directories that allows them to be read or written.
→ These attributes can also be taken away to prevent file from being read or modified.

→ R/W is a CD media first introduced in 1997. that is capable of being written to or read unlike CD-R.

Q NO 4.

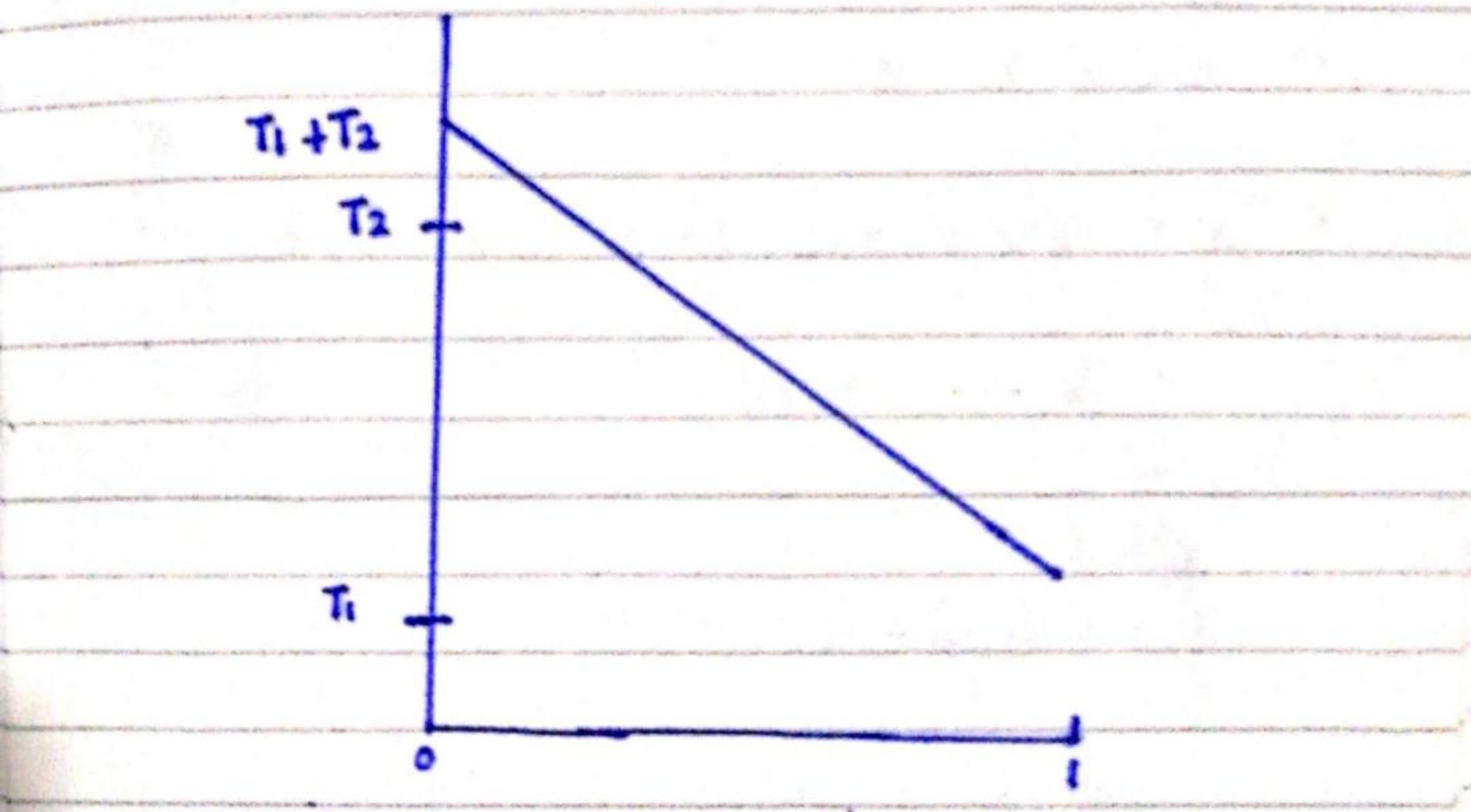
(a)

→ In our example suppose 95% of the memory access are found in level 1. Then the average time to access a word would be,

$$(0.95)(0.01\mu s) + (0.05)(0.01\mu s + 0.1\mu s)$$

$$0.0005 + 0.0055 = 0.015\ \mu s.$$

→ The average access time is much closer to 0.01 μs than to 0.1 μs as desired.



(b) (b)

→

→ Total block in the cache = 8 kbytes / 16 b =

$2^3 \times 2^{10} / 2^4 = 2^9 = 512$

→ No of set = $\frac{\text{no of block in cache}}{2}$

So,

no of set = 512/2

→ no of set in cache = 256 = 2^8

→ no of set = 8.

→ size block = 16 = 2^4

→ Size of memory = $2^6 \times 2^{20} = 2^{26}$

→ Tag = size of memory − set size of block.

= 26 − 8 − 4 = 14

set = 8

size of block = 4.

(7) (C)

→

$N = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8.$

$15 >= 12.$

		3		5	6	7		9	10	11	12
		1		1	0	0		0	0	1	0

→ Check bit 4 calculated by value in bit numbers 5, 6, 7, 12.

→ Check bit 2 calculated by value in bit num 3, 6, 7, 10, 11

→ 1 cal by no 3, 6, 7, 9, 10, 11

Check bits are 1011.

(d.)

7200 revolutions in 60 sec.

→ 1 revolution = in $\frac{60}{7200}$

→ 1 rev in 6ms.

→ 1 rev = covering one entire track = 500 sector

→ 500 sector = 6 ms,

→ 1 sector = 8 micro seconds.

Now we have,

→ 3500 sectors.

So, t = 3500 × 8 ms = 20 ms.

→ 1.28Mb = 1343177.2 bytes

= 3623 sect = 20.976 ms.

So,

Case 1 ⇒ 4+2+20 = 26 ms.

" 2 ⇒ 2+4+20.976 = 26.976 ms.