called - many integrated core (MIC)
- The multiple and MIC strategy involves a homogeneous collection of general purpose processors on a single chip.

---

GPU:- GPGPU

A GPU is a core designed to perform parallel operation on graphics data. It is found on a plug in graphics card.
- It is used to encode and render 2D and 3D graphics as well as process video.
- GPUs perform parallel operation on multiple sets of data. They are increasingly being used as vector process for a variety of application that require repetitive computations.

1) Quick Path interconnect (QPI) Protocol Layer)
In this layer the Packet is defined as the unit of transfer.

(Ans D)

Cortex - A)

The Cortex - A and Cortex - A50 are application processor intended for mobile devices such as smart phones and e book readers as well as consumer device such as digital TV and cable internet modems. These processor ran at higher clock frequency and support a memory management unit (MMU).

Cortex - R :-

The Cortex - R is designed to support real - time applications in which the timing of events needs to be controlled with rapid response to events. They can run at a fairly high clock frequency and have very low response latency.

Cortex - M :-

Coster - m series processor have been developed primarily for the micro controller domain where the need for fast highly determine interrupt

is stored in AC.

(a) The value in the PC (301) is loaded into the MAR

b) The value in Location 302 (which is the instruction with the value 2941) is loaded into the MBR and the PC is incremented

c) The value in the ~~MBR~~ MBR is loaded in to the IR.

6) a) The address (Portion of the IR (941) is loaded into the MAR.

b) The value in the AC is loaded into the MBR

c) The value in the MBR is stored in Location 941

Q.4 (Ans F)

(a) $2^{24} = 16$ MBytes

(b) (i) If the local address bus is 32 bits the whole address can be transferred at once and decoded in memory However, because the data has

- RU ( Recovery unit)
  The RU keeps a copy of the complete state of the system that includes all registers, caches, hardware, fault signal etc.
- CoP
  The CoP is responsible for the data compression and encryption function for each etc.
- I - cache
  This is a 64-kB L1 instruction each allowing IFU to prefetch instruction before they are needed.
- L2 Control
  This is a control logic that manages the traffic through the two ~~managers~~ L2 caches.

---

Data L2
A 1- mB data cache for all memory traffic other than instruction.

Instr - L2 :
A 1- mB L2 instruction each.

---

- Memory Latency and Throughput.
  Memory ~~increase~~ access speed (latency) and transfer speed. Through put lag processor speeds.

---

(6) Consider a program runing on a single processor such that a fraction (1-f) of the execution that a function code that is inherently sequential and a function of that involves code is infinitely parallelizable with no scheduling overhead. Let T be the total execution time of the program using a single processor, Then the speed up using a parallel ~~increa~~ ~~portion~~ of the program processor with N processor that fully exploits the Parallel Portion of the program is as follows.

Speed up. Time to execute Program on a single Processor

Time to execute Program On N Parallel processor.

Speed up $= \frac{T(1-f)+Tf}{T(1-f+\frac{Tf}{N}} = \frac{1}{1-f+f/N}$.

(11) Multicore:

The use of multiple processor on the same chip. also referred to as multiple Cores. or multicore also referred to the potential to increase performance with out increasing the clock rate.

If the software can support the effective use of multiple processor then doubling the number of processor almost double performance. Two core chips were quickly followed by four-Core chips then 8, then 16, and so on.

---

(11C)

The leap on performance as well as the challenge in developing software to exploit such a large number of Cores has led to the introduction of new term

The technique used in Contemporary processors to increase speed are following.

- Pipelining: This enables a processor to work simultaneously on multiple instruction by performing a different phase each of the multiple instruction at the same time.
- Branch Prediction.
  Branch prediction potentially increase the amount of work available for the processor to execute.
- Super scalar Execution:
  This is the ability to issue more than one instruction in every processor clock cycle. In effect multiple parallel piplines are used.
- Data flow analysis:
  The processor analyze which instruction are dependent on each other's result or data to create an optimized schedule of instruction.

* Speculative execution :-
This enables the processor to keep its execution engines as busy as possible by executing instruction that are likely to be needed.

Ans f) The problems created due to increase in clock speed and logic density of the processor are.

Power :- As the density of logic and the clock speed on a chip increase, so does the Power density the difficulty of dissipating the heat generated on high density high speed chips is becoming a serious design issue.

R C Delay :-
The speed at which electrons can flow on a chip between transistor is limited by the resistance and capacitance of the metal wires connecting them specifically delay increase as the RC product increase.

Ans c) Embedded System :-

The term embedded system refers to the use of electronics and software with in a product as opposed to a general purpose computer such as laptop or desktop system. Today many devices that use electronic power have an embedded computing system.

Different embedded system used in everyday life are cell phones, digital cameras, video cameras, calculator microwave ovens. home security system

Ans D) Different desktop application that require the great power of contemporary microprocessor based system.

- image processing
- three-dimensional rendring
- speech recognition
- video conferencing.
- multimedia authority
- voice and video anotation of field
- Simulation modelly.

1) IAS operation.

The IAS operation by repetively performing an instruction cycle. Each instruction cycle Consists of two subcycles.

1: fetch cycle:

During fetch cycle the opcode of the next instruction is loaded into the IR and the address portion is loaded into the IR and the MAR. This instruction may be taken from the IBR. or it can be obtained from memory by loading a word into the MBR and Then down to the IBR and MBR

---

Execute Cycle:

Control Circuitry interpret the opcode and executes the instruction by sending out the appropriate control signal to cause, data to

---

be moved or an operation to be performed by the ALU.

- LSU: ( Load Store unit)
  It is responsible for handling all types of operand access of all lenght modes and formulas as defined in the z/Architecture.

---

- XU ( Translation Unit)
  This unit translates logical address from instruction into physical address in main memory.

FXU ( Fixed Point Unit)
The FXU executes fixed point architecture operation.

BFU ( Binary Floating Point Unit)
The BFU handles all binary and hexadecimal floating point operation as well as fixed point multiplication operation.

---

DFU Decimal Floating Point Unit.
The DFU handles both fixed Point and floating operation on number that are stored as decimal digits.

---

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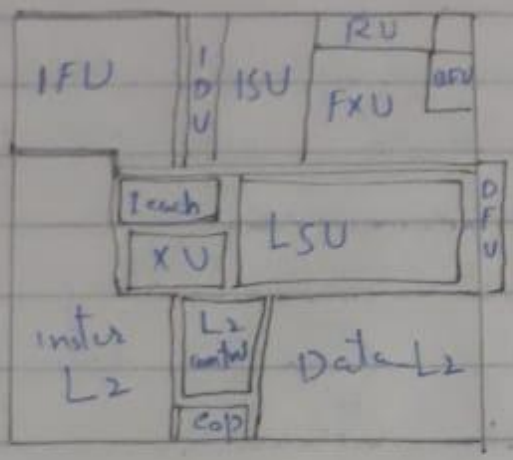
(Q no. 1)




Function of each Sub area:

- ISU ( instruction Sequence Unit.)

Determine the sequence in which instruction are executed in what is refereed to as a Superscaler architicture.

- IFU ( instruction fetch Unit)

Logic for fetching unit.

- IDU: ( Construction decode Unit)

The IDU is fed from the IFU buffers and is responsible for the prasing and is responsible for the architecture operation codes.

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Paper. Computer architecture.

$T_8 = 1.8$ ms

speed up = 11/1.8.

(d)

By depending on the information given it is not obvious have to quantify thus effect in Amdah's equation, Therefore it is supposed that the fraction of code which is Parallizable is $f = 1$ then Amdah's decreases to speed-up = $N = 8$ Therefore. The out of speed up is only 75%. of the theoretical speed up.

The END

(Q: 4 Part d)

| instruction type | CPI | instruction. mix |
|---|---|---|
| Arthemetic & logic | 1 | 60% |
| Load / store with cache hit | 2 | 18 %. |
| Branch. | 4 | 12 %. |
| memory reference with cache miss | 12 | 10 %. |

The average CPI = (1 × 0.6) + (2×0.18) + ( 4×0.12 + (2 × 0.1) = 2.64

Therefore CPI has been increased Since The time for memory accen is also increamed

(b) mips = 400 / 2.64 = 152

There is corresponding drop in the mips rate

(c) T = Ic (mips x $10_6$)

for the One Processor).

$T_1$ = (2 x $10_6$) / 178 x $10_6$) = 11 ms

For the processor each processor execute 1/8 if the 2 million instruction Plus the 25,000

(Part c)

(7) etic CPI's

$CPI = (1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 9000) / 100$

$CPI = 162000 / 100$

$CPI = 1620$

MIPS

mips rate = 60 mHz / $1620 \times 10^6$

mips rate = $60 \times 10^6$ Hz / $1620 \times 10^6$

= 60Hz / 1620

mips rate = 0.037

Execution Time :

$I = Ic / (MIPS \times 10^6)$

$T = 104000 / (0.037 \times 10^6)$

$T = 104000 / 37 \times 10^6$

$T = 2811 \times 10^{-3}$

$T = 2.811$ Sec

(Q4 Part B)

(a) opcode 000000d
operand 0000000000010

(b) In the beginning the CPU have to fetch the instruction from the memory, then the instruction will include the address of the data which is required to load. Through the execution time, the memory will be accessed in that time to load the data contents which is located at that address for a total of two trips to memory.

in only 16 bits. It will require 2 cycle to fetch a 32-bit instruction or operand.

2) The 16 bit of the adress placed on the adress bus can't access Complex memory. Thus, a more complex memory interface control is needed to Latch the first part of the address and then the second part.

c) The Program Counter must be at least 24 bits. Typically a 32 bit microprocessor will have a 32-bit external address bus, and a 32 bit Program Counter. unless On chip segment register are used that may work the instruction register is to contain the whole instruction. it will have to be 32-bit long. it will Contain only the Op code (called the op code register then it will have to be 8 bits long.

is loaded into the IR.

2) a) The addres portion of the IR (940) is loaded into the MAR
b) The value in location 940 is loaded into the MBR.
c) The value in the MBR is loaded into the AC

3) a) The value in the PC (301) is loaded into the MAR.
b) The value in location 301 (which is the instruction with the value 5941) PC is incremented.
c) The value of in the MBR is loaded into the IR.

4) a) The addres portion of the IR (941) is loaded into the MAR
b) The value in location 941 is loaded into the MBR.
c) The old value of the AC and the value of location MBR are added and the result

(Q NO. 4) (G)

A bus cycle takes 0.25 μs so a memory cycle take 1 μs. if both operands are even aligned. it takes 2 μs to fetch the two operands. If one is odd aligned the time required is ~~odd~~ 3 μs. if both are odd aligned the time required is 4 μs.

(Ans E)

Six steps.

① The PC contains 300. the address of the first instruction. This value is loaded into the MAR

② The value in location 300 (which) is the instruction with the value of 1940 in hexadecimal is loaded into the MAR and the PC is incremented These two steps can be done Parallel ③ The value in MBR is

RH instruction;;

21 = 00100001 = STOR (m(x)

m(x) = refers to the memory address Location OFB

The second 5 bits of 08c Should read - STOR m(OFB)

Finally the assembly language code for 08c 0L0 FA1 OF B is

LOAD -m(OFA)

STOR (m(OFB)

1) In 08A address the m(OFA) transfer to the accumulator and transfer contents of accumulator to memory location OFB.

In 08B adress The m(OFA) transfers to the accumulator and take next instruction from Left hast of m(08D).

In 08c adress The m(OFA) transfer to the accumulator and transfers contents of accumulator to memory

Location OFB

Here is Simple way to understand this problem

Contents are divided up into two bit 5 bit instruction LH and RH

LH instruction = 01 0FA

opcode = 01

address = 0FA

RH instruction = 0F 08 D.

Contents are divided upto two 5 bits instruction LH and RH

LH instruction 02 0FA

opcode = 02

address = 0FA

RH instruction = 21 0FB

opcode = 21

address = 0FB.

LH Instruction ;

02 = 00000010 = LOAD - M(X)

M(X) refers to the memory address location 0FA.

The first 5 bits of 08 should read Load M(0FA).

opcode = 01
adress = 0FB

Since this is hexadecimal from you have to convert this number to binary from.

LH instruction ;;

01 = 0 0000001 : LOAD M(x)

M(x) refers to the memory adress Location of A

the first 5 bits of 08A should read - LOAD M(0FA)

RH instruction ;;

21 = 00100001 . Stor M(x)

M(x) refers to the memory adress Location = 0FB

Th Second 5 bits of 08A should read - Stor (M)(0FB)

Finally the assembly language code for 08A 01 0FA 21 0FB is

LOAD (M(0FA)
STOR M(0FB)

Programming in Software:

The new method of Programming which is a sequence of codes or instructions is called Software Programming. In this method Programming is much easier instead of rewing the hardware for each new programe all we need to do is provide a new sequence of codes each code is in effect an instruction and part of the hardware interups each instruction and generate Control Signal.

---

Q:NO: 4

(A) (a)

1. Here is Simple way to understand this problem Contents are divided up into two 5 bits instruction LH and RH

LH instruction: 01 0F A.

checked by the processor after the processor has enabled interups when a user program is executing and an interupt occurs interups are disabled immediately.

---

Nested interrupt :-

Nested interrupt is to allow interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted. A user program begins at t=0. At t=10, a printer interrupt occurs. User information is placed on the system stack and execution continues at the printer interrupt Services routine (ISR) while this routines Services is still executing at t = 15, a Communication interrupt occurs.

---

management is coupled with the desire for externally low gate count and lowest possible power consuption.

(Ans E)

In the interupt cycle, the processor checks to see if only interups have occured indicated by the presence of an interupt signal. If no interups are pending the processor proceeds to the fetch cycle and fetches the next instruction of the current Program.

(Ans F)

Disabled interupt:

A disabled interupt simply means that the processor can and will ignore that interups request signal if an interupt occurs during this time. It generally remains the pending and will be

(Ans C)

Microprocessor :-

A microprocessor chips included register on ALU and some sort of control unit Or instruction procesing logic As transistor desity increased it became possible to increase the complexity of the instruction set architecture and ultimately set Architecture and ultimately to add memory and more then one procesor chips include multiple Cores and substantial amount of cache memory.

---

MicroController :-

A microcontroller is a single chip that contains the procesor non-volatile memory for the program (Rom) vollatile memory for input and output (RAM) a clock and an I/O Control unit. The procesor portion of the microcontroller has a much lower Silicon area Than other microprocessor and much higher energy efficiency.

of design effort on
Complex instruction Set:

Cisc The x86 incorporate the sophisticated design principles once found only on main frames and super Computer and serves as an excellent example of Cisc design.

Risc:
An alternative approach to processor design is the reduced instruction set Computer. (Risc)
The ARM variety of embedded is used in a wide variety of embedded system and it is one of the most powerful and best designed Risc.
Based system on the market
In this Section and the next we provide a brief overview of these two systems.

Q no. 3

(Ans A)

Computer architecture:

Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program. A term that is often used interchangeably with Computer architecture is instruction set architecture (ISA).

Computer organization:

Computer organization refers to the operational units and their interconnections that realize the architectural specification.

Example of Architectural attributes include the instruction set the number of bits used to represent various data types (e.g. numbers) I/O mechanism and techniques for addressing memory.

---

(CISC) The Current x86 offering represents the result of decades

Data lines:
The data lines provide a path for moving data among system modules. These lines collectively are called the data bus. The data bus may consist of

- Adress Lines.
The adress lines are used to designed the source or destination of the data on the data bus. The width of the adress bus determines the maximum possible memory capacity of the system.

→ Control lines:
The control lines are used to control the access the and the use of the data and adress lines. Because the data and address there must be a means of controlling their use, typically control include.

memory write, memory read, I/O write I/O read and etc.

Hardware failure :
It is generated by a failure such as power failure or memory parity error.

(Ans! G.)

Bus interconnection Scheme :
The most common computer interconnection structures are based on the use of one or more system buses.
A system bus exists typically of about fifty to hundreds of separate lines the lines can be classified into three functional group. data adress and control lines.

Data lines :
The data lines provide a path for moving data among system modules, these lines collectively are called the data bus.
The data bus may exists of of 32, 64, 128, or even more separate refered to as width of data bus.

Data operand (do):
Perform the operation indicated in the instruction.

- Operand store (os):
write the result into memory or out to I/O.

(Ans F)

Clases of interups:;

- Program:;
It is generated by some condition that occurs as a result of an instruction execution such as arthmatic overflow, division by zero attemp to execute an illegeal machine instruction or reference outside a user's allowed memory space.

Timer:;
It is generated by a timer with in the processor, This allows the operating request service from the processor, or to signal a variety of error condition.

Ans (c)

Instruction cycle state Diagram:

The States in instruction cycle state diagram are follows

- Instruction address calculation (iac)
  Determine the address of the next instruction to be executed usually this involves adding a fixed number to the address of the previous instruction.
- Instruction fetch (if):
  Read instruction from its memory location onto the processor.
- Instruction operation decoding (iod)
  Analyze instruction to determine type of operation to be performed and operand to be used.
- Operational adress calculation (oac)
  If the operation involve reference to an operand in memory or available via I/O then determine the adress of the operand.
  Operation fetch (of):
  fetch the operand from memory or read it in the from I/O

Ans (c)

Stored Program Computer:

A fundamental design approach first implemented in the IAS Computer is known as the "stored Program concept". This idea is usually attributed to the mathematician John Von Neumann. The first Publication of the idea was in a 1945 Proposal by Von Neumann's for a new Computer The EDVAC (Electronic Discrete variable) Computer.)

In 1946, Von neumann and his colleagues began the design of a new stored Program Computer referred to as the IAS. Computer at the princeton institute for advanced studies, it consist of.

=> A main memory Which Stores both data and instruction.

=> An arithmatic and Logic Unit (ALU) capable of operating binary data.

Ans 13. The characteristics of Computer family are as follows.

- Similar or identical instruction set:
  In some cases the lower end of that is a subset of that of the top end of the family this means that programs can move up but not down.
- Similar or identical operating system:
  The some basic operating system is available for all family member.
- Increasing Speed:
  The rate of instruction execution increases in going from lower to higher family members
- Increasing number of I/O Ports:
  The number of I/o ports increases is going from lower to higher family member.
- Increasing memory Size:
  At a given in time the cost of a system increases in going from lower to higher family members.

(Ans D)

Moore's Law:-

The famous Moor's law which was proposed by Gordon moor's Co-founder of intel, in 1965, moore observed that the number of transistor that could be put on year and correctly predicted that this place would continue into the near future.

The Consequences of moor's law are

The cost of Computer logic and memory circuitry has fallen at a dramatic rate

The Computer become smaller making, it more convenient place in a variety of environment.

The is a reduction in power requirement.

The interconnection on the integrated circuit are much more variable then solder connections.

2 main memory
   It stores data.

3- Q no: 2
   Ans (A)

Structural components of computer:
There are four main structural components of Computer.

1) Central processing unit (CPU).
   It Controls the operation of the computer and performs its data processing function often simply referred to as processor.

2- Main Memory:
   It stores data.

3- I/O: It moves data between the computer and its central equipment.

4- System interconnection:
Some mechanism that provides for communication among CPU main memory and I/O. A common example of System interconnection is by means of a System bus.

PCIe links from the chipset may attach to the following kinds of devices that implements PCIe.

* Switch:
  The switch manages multiple PCIe streams.
* PCIe endpoint
  An I/O device or Controller that implements PCIe.
  Such as a gigabit ethernet switch or graphics, disk, interface, etc
* Legacy endpoint
  Legacy endpoint category is intended for existing designs that have been migrated to PCI express and it allows legacy behaviours. Such as use of I/O space and Locked transaction.
* PCIe / PCI bridge
  Allow older PCI devices to be connected to the PCIe-based system.

* The Packet Contents definition is standardized with some flexibility allowed to meet differing market segment requirement.
* One key function performed at this layer is a Cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent.

1) Physical and logical Architecture of PCIe:

Root Complex:

It is also called chipset or a host bridge which connects the processor and memory sub system to the PCI express switch fabric comprising one or more PCIe and PCI switch devices.

The root complex acts as a buffering device to deal with difference in data rates between I/O controllers and memory and processor components.