Name::Daniyal Alam

ID ::15385

DLD LAB FINAL

TEACHER ::SIR AMIN

Question #1

Part “A”

Design and verify the logic circuit of Half adder using logic gates.

OBJECTIVES:

- To understand the principle of binary addition.
- To understand half adder concept.
- Use truth table and Boolean Algebra theorems in simplifying a circuit design.
- To implement half adder circuit using logic gates

PROCEDURE:

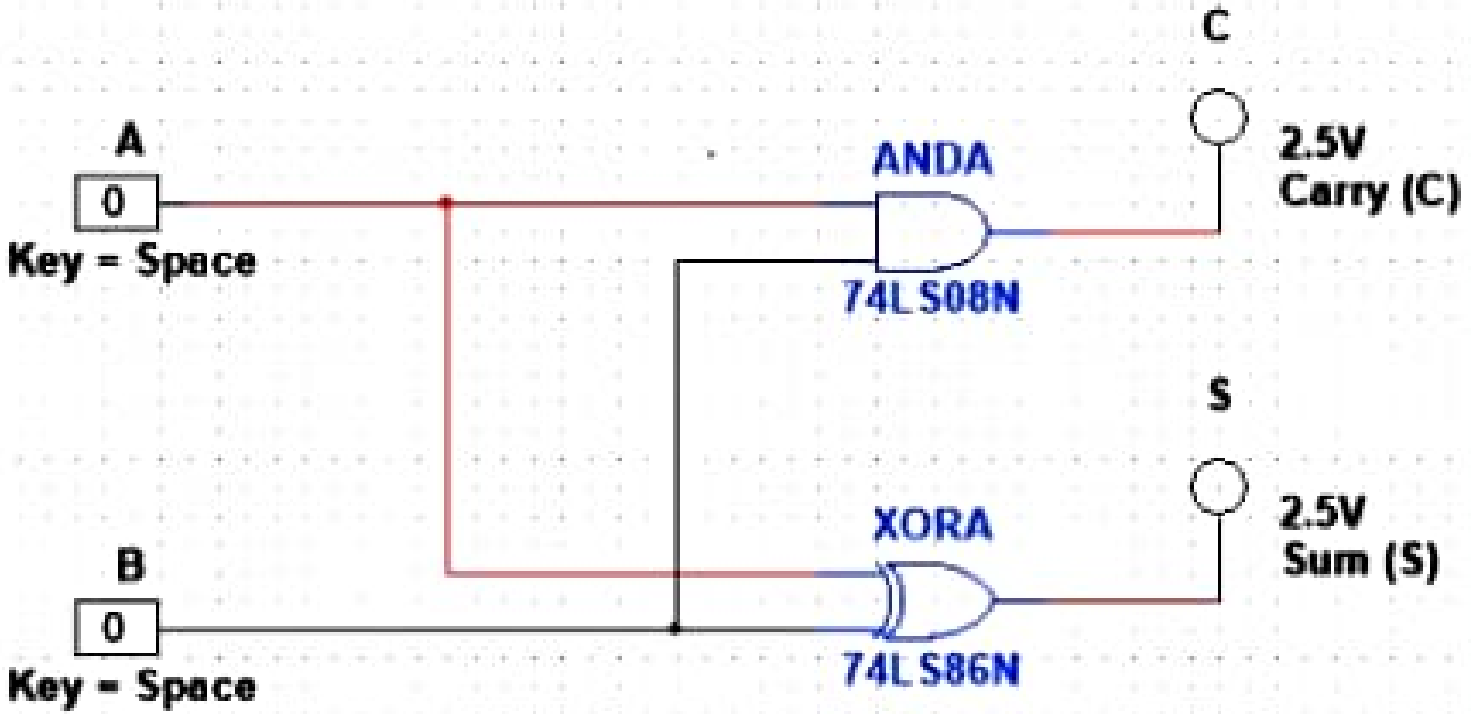
1. collect the components necessary to accomplish this experiment.
2. Plug the IC chip into the breadboard.
3. Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V.
4. According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
5. Connect the inputs of the gate to the input switches of the LED.
6. Connect the output of the gate to the output LEDs.
7. Once all connections have been done, turn on the power switch of the bread-board
8. Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs.

HALF ADDER:

Half Adder: A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.

OBSERVATION TABLE:

Inputs		Outputs	
A	B	SUM (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1


C
A
2.5V
Carry (C)
ANDA
0
Key = Space
74LS08N
S
2.5V
Sum (S)
XORA
B
0
Key = Space
74LS86N

RESULTS AND ANALYSIS:

Half Adder: Verified the truth table of Half Adder as S = 1 i.e. LED which is connected to S terminal glows when inputs are A, B Verified the truth table of Half-Adder as C = 1 i.e. LED which is connected to C terminal glows when inputs are A, B.

CONCLUSION:

- **To add two bits we require one XOR gate(IC 7486) to generate Sum and one AND (IC 7408) to generate carry.**
- **To add three bits we require two half adders.**

Question #1

Part “B”

Design and verify the logic circuit of Half-subtractor using logic gate.

OBJECTIVES:

- To understand the principle of binary subtraction.
- To understand half-subtractor concept.
- Use truth table and Boolean Algebra theorems in simplifying a circuit design.
- To implement half-subtractor circuit using logic gates

PROCEDURE:

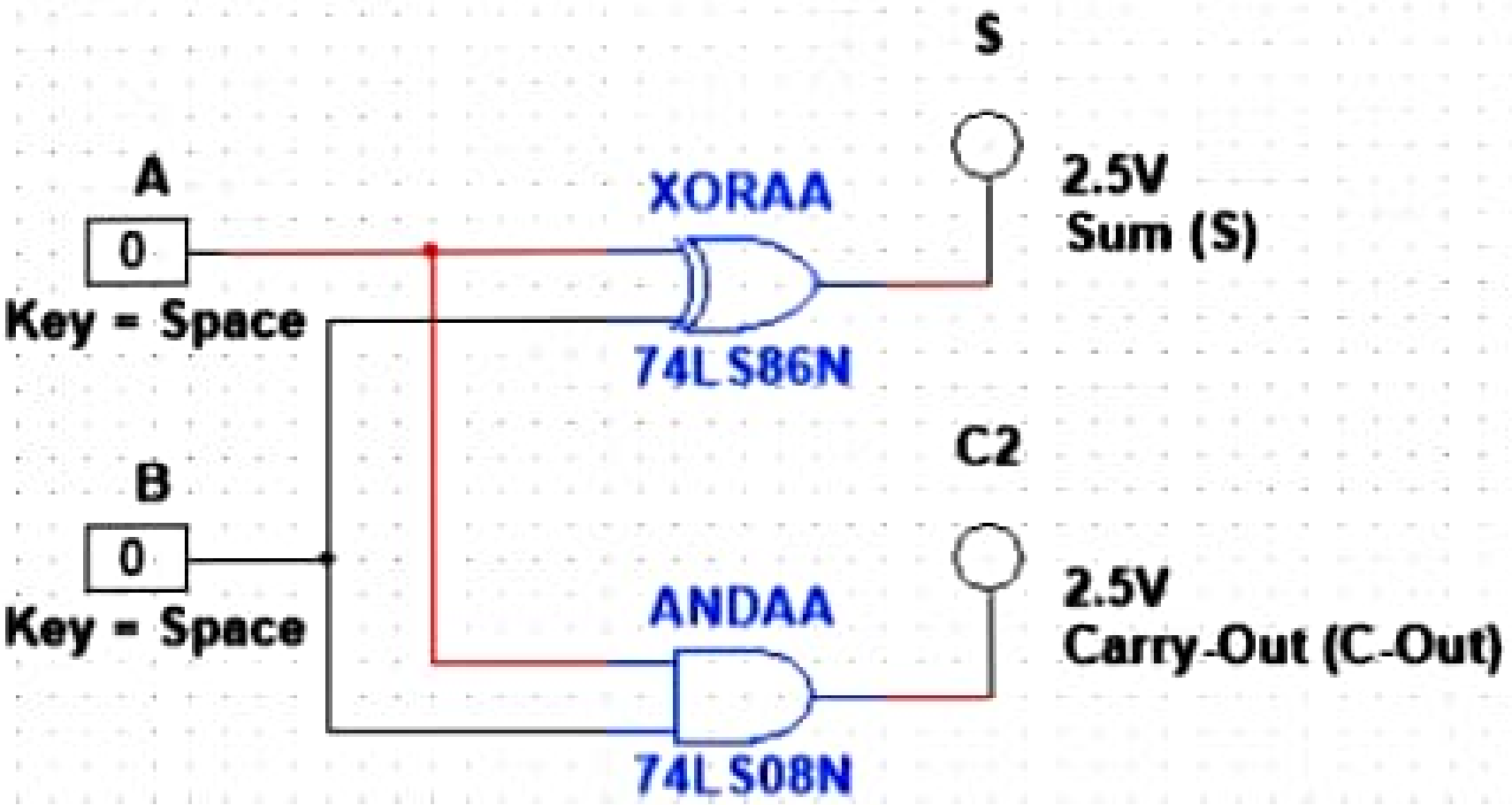
- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V.
- According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of the bread-board
- Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs.

HALF SUBTRACTOR:

The half-subtractor is a combinational circuit which is used to per-form subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

OBSERVATION TABLE:

A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0


S
A
0
Key = Space
XORAA
2.5V
Sum (S)
74LS86N
C2
B
0
Key = Space
ANDAA
2.5V
Carry-Out (C-Out)
74LS08N

RESULTS AND ANALYSIS:

Verified the truth table as follows.

Verified the truth table of Full Subtractor as D = 1 i.e. LED which is connected to D terminal glows when inputs are, Y, BIN Verified the truth table of Full Subtractor as BOUT = 1 i.e. LED which is connected to BOUT terminal glows when inputs are X, Y, BIN

CONCLUSION:

- **To add two bits, we require one XOR gate (IC 7486) to generate Difference and one AND (IC 7408) and NOT Gate (IC 7432) to generate Borrow.**
- **To add three bits, we require two half subtractor.**

Question #1

Part “C”

To Design and verify the truth table of J K Flip flop

OBJECTIVES:

- To understand the principle of operation of sequential circuit
- To differentiate between combinational circuit and sequential circuit.
- To get familiar with basic Flip flops
- Determine the logic operation of JK flip flops.
- Connect and observe the state transition of JK as connected to the clock generator circuit.

PROCEDURE:

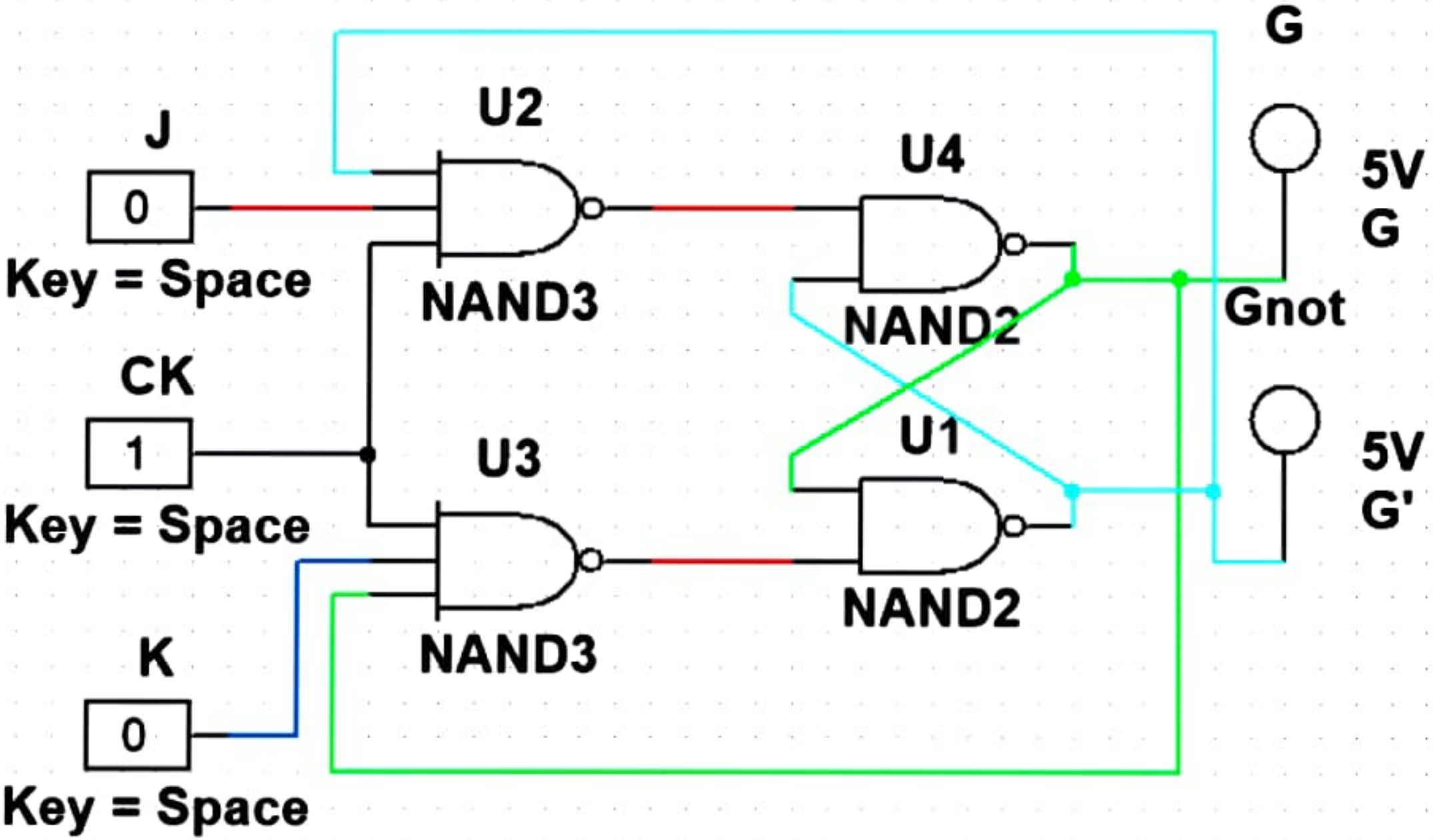
- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V.
- According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of the breadboard
- Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs.

JK Flip Flop:

A flip-flop is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs

Observation Table:

CK	J	K	Q	$\overline{Q}$
1	0	0	-	-
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1


G
J
U2
U4
5V
G
0
Key = Space
NAND3
NAND2
Gnot
CK
1
Key = Space
U1
5V
G'
U3
NAND2
NAND3
K
0
Key = Space

Results and Analysis:

Flip-flops (FFs) are devices used in the digital field for a variety of purposes. Flipflops are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. In JK flip-flop, the letter J is for set and the letter K is for clear. When logic 1 inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa. Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs.) It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Conclusion:

The function table of JK flip flop using IC 7473 has been verified.

Question #1

Part “D”

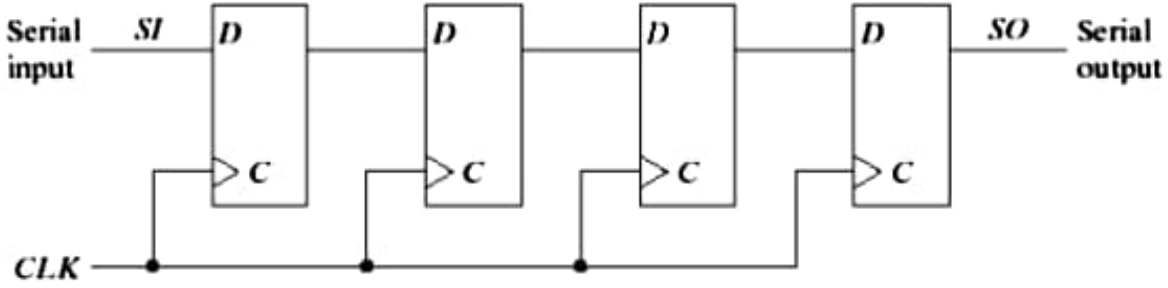
OBJECTIVES:

To investigate the operation of the shift registers.

BACKGROUND:

A register capable of shifting its binary information either to right or to the left is called a shift register. The simplest possible shift register is one that uses only flipflops,

The Q output of a given flip-flop is connected to the D input of the flip-flop at its right. Each clock pulse shifts the contents of the register one-bit position to the right. The serial input determines what goes into the leftmost flip-flop during the shift. The serial output is taken from the output of the rightmost flip-flop prior to the application of a pulse. Although this register shifts its contents to the right, if we turn the page upside down; we find that the register shifts its contents to the left. Thus, a unidirectional shift register can function either as a shift-right or as shift-left register.


Serial input
SI
D
C
D
C
D
C
D
C
SO
Serial output
CLK

CLK	Q0	Q1	Q2	Q3
Initial	0	0	0	0
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	0	1	0

DISCUSSION:

Excess-3 code is a 4-bit un-weighted code and can be obtained from the corresponding value of BCD code by adding three to each coded number. Excess-3 code is self-complementing in nature because 1â˘AZ´ s complement of the coded number yields complements of number itself.

CONCLUSION:

various types of shift register have been implemented and verified using ICs.

Question #1

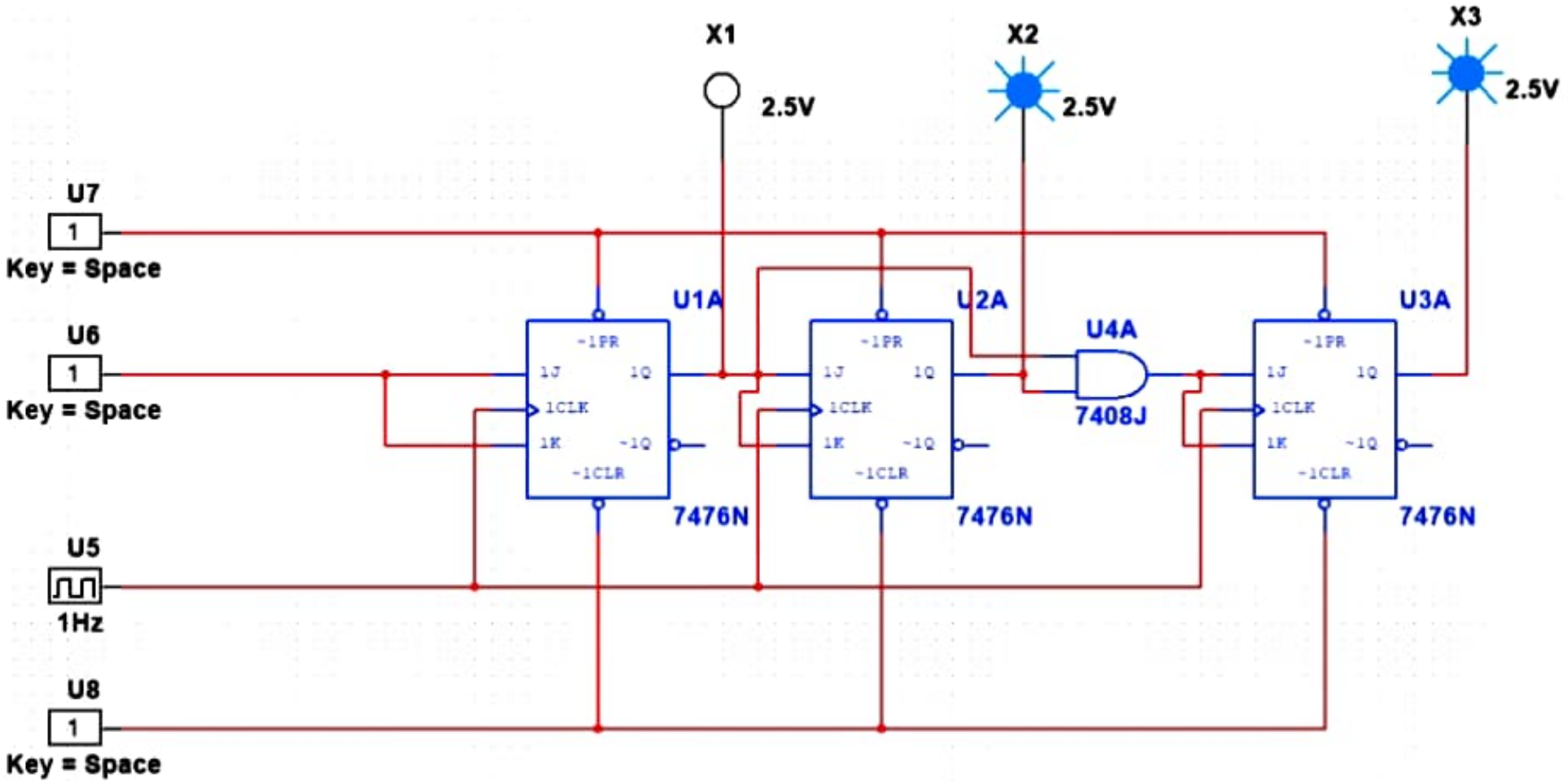
Part “E”

AIM:

Realization of 3-bit synchronous counter design.

PROCEDURE:

- **Connections are made as per circuit diagram.**
- **Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.**
- **Verify the Truth table.**


X1
2.5V
X2
2.5V
X3
2.5V
U7
1
Key = Space
U6
1
Key = Space
U5
1Hz
U8
1
Key = Space
U1A
U2A
U4A
U3A
7408J
7476N
7476N
7476N
~1PR
1J
1Q
1CLK
1K
~1Q
~1CLR

CLK	Q_0	Q_1	Q_2
Initial	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (Recycles)	0	0	0

CONCLUSION:

03-bit synchronous counter has been implemented and verified using ICs.