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Assignment #4

Q1

i)

Ans:- An access time become faster the cost per bit increase As memory size increase, the cost per bit is smaller. Also with greather capacity. the access time become slower.

ii)

Ans:- Another distination among memory types is the method of accessing units of data. these include the following.

Sequential access:-

Memory is organized into unit of data called records Access must be made in a specific linear sequence. Stored addressing information is used to seperate records & assist in the retrieval Process. A shared read-write mechanism is used & this must be moved form it current location to the desired location, Passing & rejecting each information record.

Direct access:-

Each addressable location in memory has a location in memory has a unique

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Random Access:

Each addressable location in memory has a unique, physically wired-in addressing mechanism. the time to access a given location is independent of the sequence of prior accesses & is constant. thus any location can be selected at random & directly addressed & accessed.

Associative:

This is a random access type of memory that enables one to make a comparison of desired bit location with in a word for a specific match. & in to do for all words simultaneously.

iii)

Slower & less expensive memory is used in higher stages, with the most expensive being the registers in the processor as well as cache. main memory is slower & less expensive.

iv)

Direct mapping:-

The simplest technique maps each block of main memory into only one possible cache line

Associative mapping:-

Permits each main memory block to be loaded into any line of the cache

Set Associative map:-

A compromise that exhibits the strength of both the direct & associative approaches while reducing their ~~dis~~ disadvantages.

Q2

i)

Unit of transfer:-

It is the maxium number of bits that can be read or written into the memory at a time.

ii)

Memory Performance Parameters:-

The two most important characteristics of memory is capacity.

Three Performance Parameter are used.

Access time (latency): for random access memory this is the time it take to perform a read or write operation. that is the time from the instant that an address is presented to the memory to the instant that that data have been stored or made available for use.

Memory Cycle time: This concept is primarily applied to random access memory & consist of the access time plus any additional time required before a second access can commence.

Transfer Rate: This is the rate at which data can be transfered into or out of a memory Unit.

iii) Disk Caches:-

A Portion of main memory can be used as a buffer to hold data temporarily that is to be read out to disk.

iv) Principle of locality:-

The Principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

v) logical Cache & Physical Cache:-

A logical cache is also know virtual cache
A Physical cache Store data using main memory Physical addresses.

vi) Replacement Algorithms:-

Once the Cache has be filled, when a new block is brought into the Cache, one of the existing blocked must be

Hardware transparency:-
Additional hardware is used to ensure that all update to main memory via cache are reflected in all caches.

Q3
i) Sequential:-
Memory is organized into unit of data called records. Access must be made in a specific linear Sequential.

direct:-
As with Sequential access, direct access involves a shared read-write mechanism, However, individual blocks or record have a unique address based on physical location.

Random access:-
Each addressable location in memory has a unique physical wired-in address mechanism.

associative:-
With associative mapping there is flexibility as to which block to replace when a new block is read into the cache.

ii) Set associatives-

mapping is a technique that exhibits the strengths of both the direct & associative approaches while reducing their disadvantages.

iii) Split Cache & Unified Cache:-

Has become common to Split Cache.

⇒ one directed to instruction
⇒ one directed to data

iv) Write through & write back-

Write through

Simplest technique

All write operations are made to main memory as well as to the cache.

Q4

i)

Suppose 95% of memory accesses are found in level 1.

then the ~~advantage~~ average time to access time is much closer to 0.01 ms than to 0.01ms as desired.

used.

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ii)

There are a total of 8kbyte/16 byte = 512 lines in the Cache.

Main memory address

Tag Set word