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Course Codes: CSC-201

EDP Codes: 102002078

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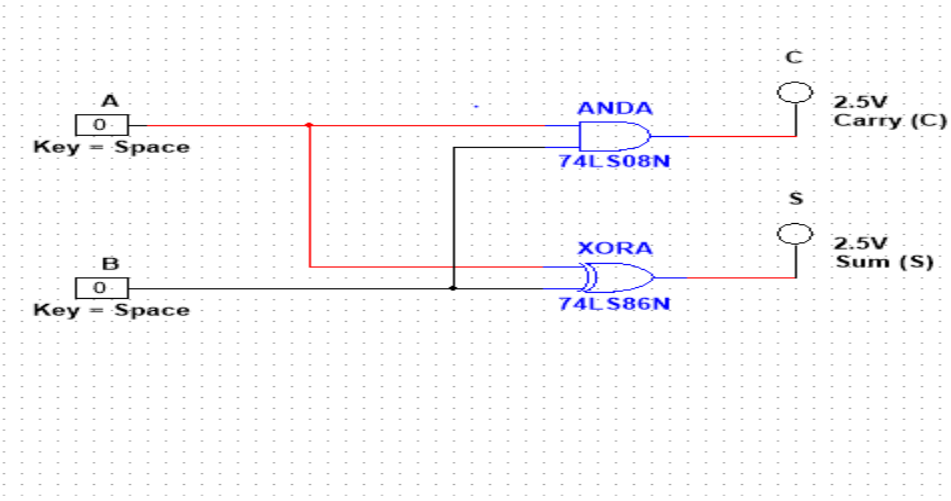
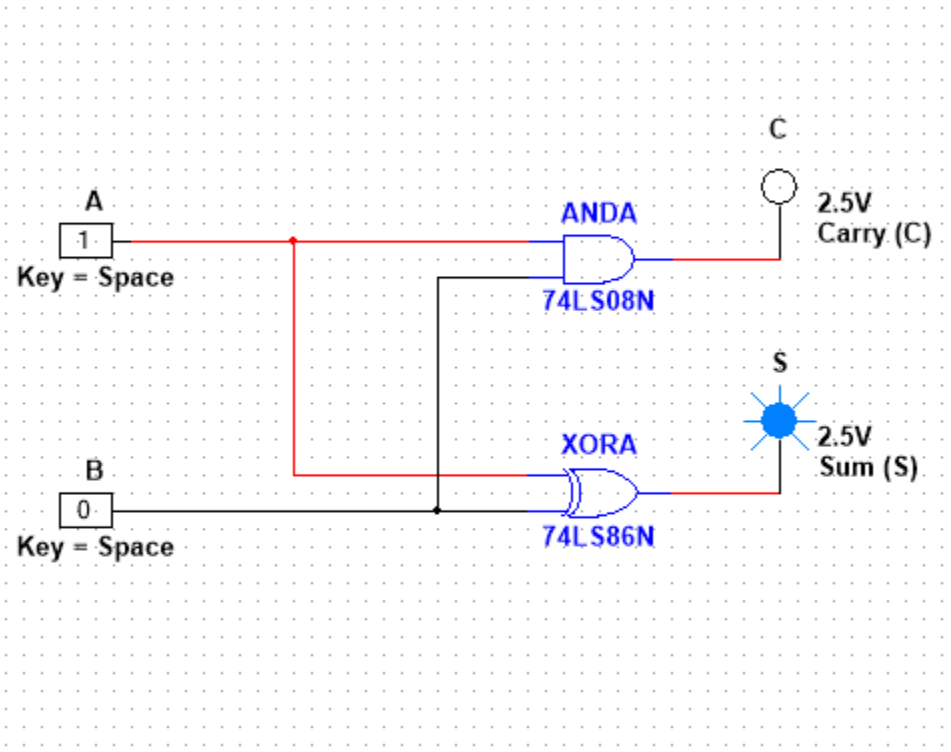
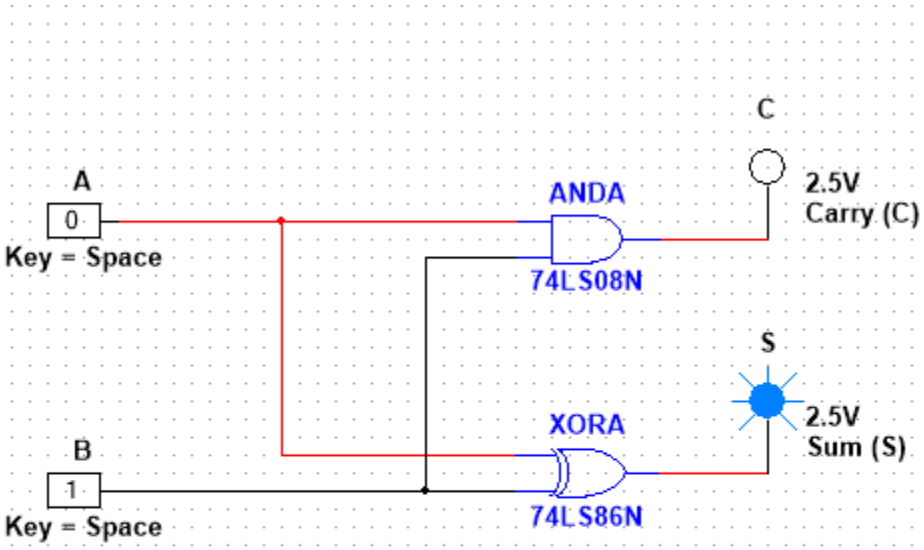
**Note: Use MultiSim to design the following circuits. Use truth tables where necessary.**

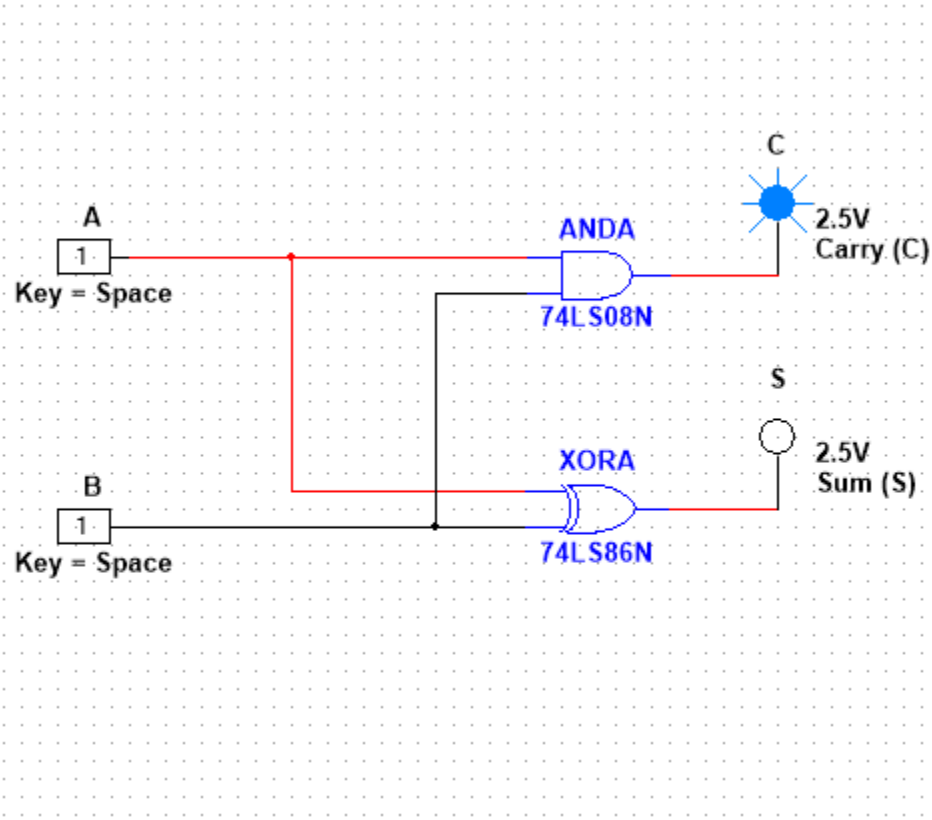
**Q.1 Design and verify the logic circuit for the following:**

**(a) Half adder using logic gates**



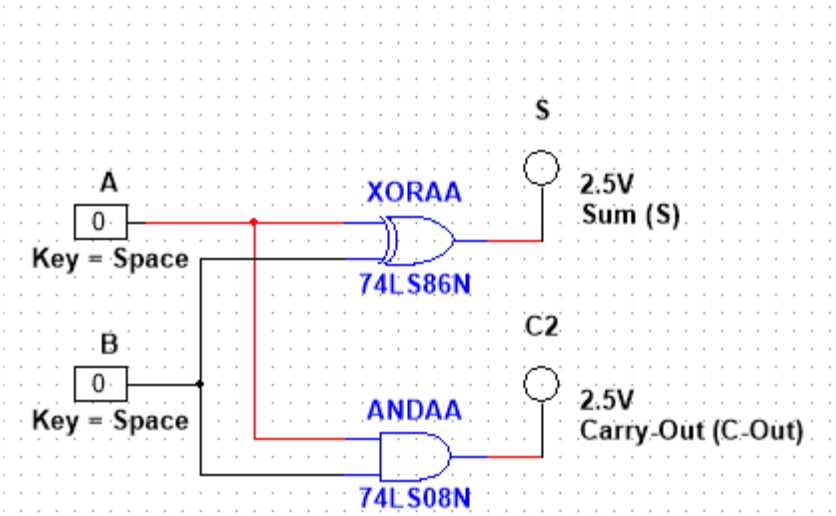

C
A
0
Key = Space
ANDA
74LS08N
2.5V
Carry (C)
S
XORA
2.5V
Sum (S)
B
1
Key = Space
74LS86N

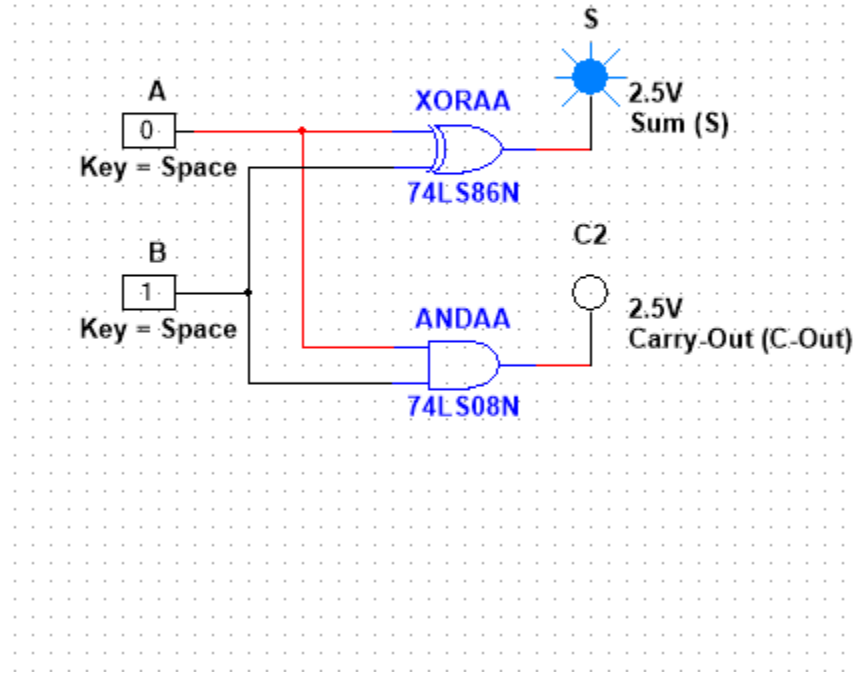

C
A
1
Key = Space
ANDA
74LS08N
2.5V
Carry (C)
S
XORA
2.5V
Sum (S)
B
1
Key = Space
74LS86N

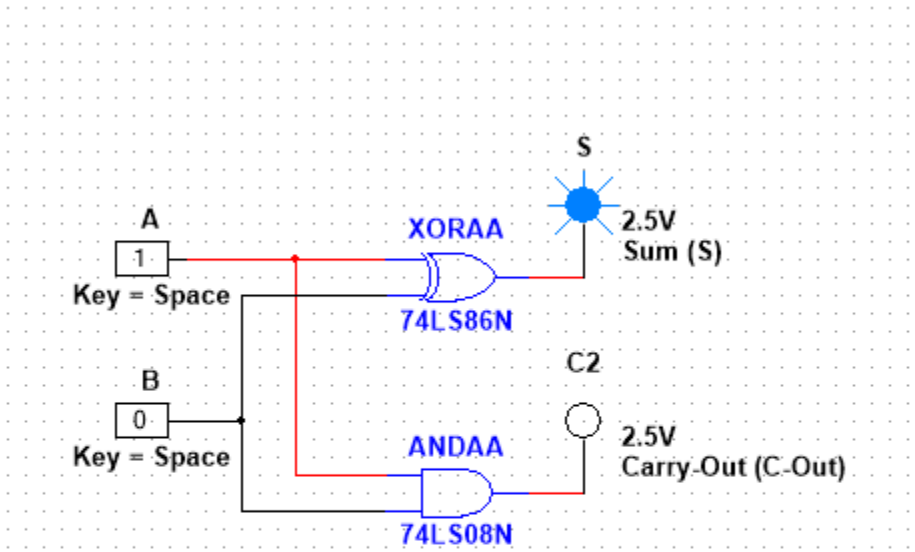
Truth Table

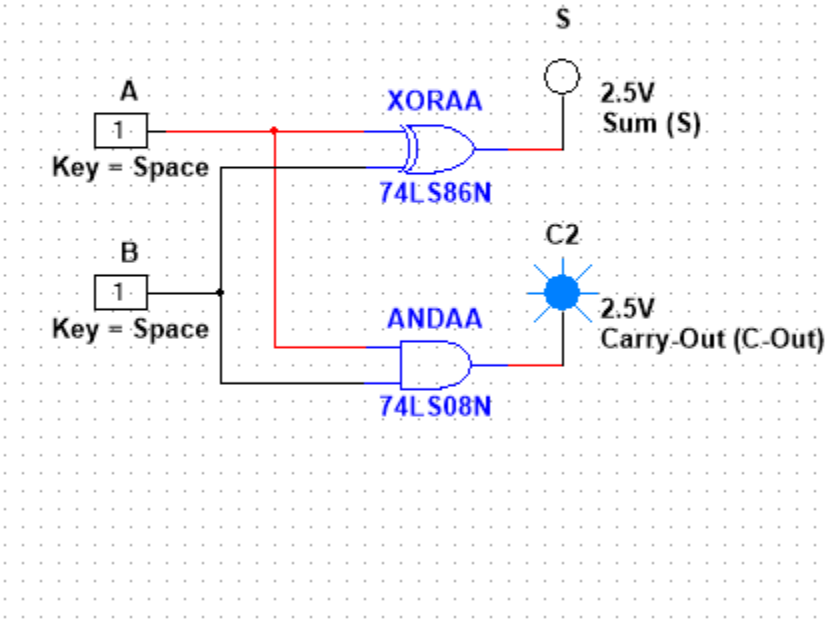
| Inputs | | Outputs | |
|---|---|---|---|
| A | B | SUM (S) | Carry (C) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**(b) Half-subtractor using logic gate**



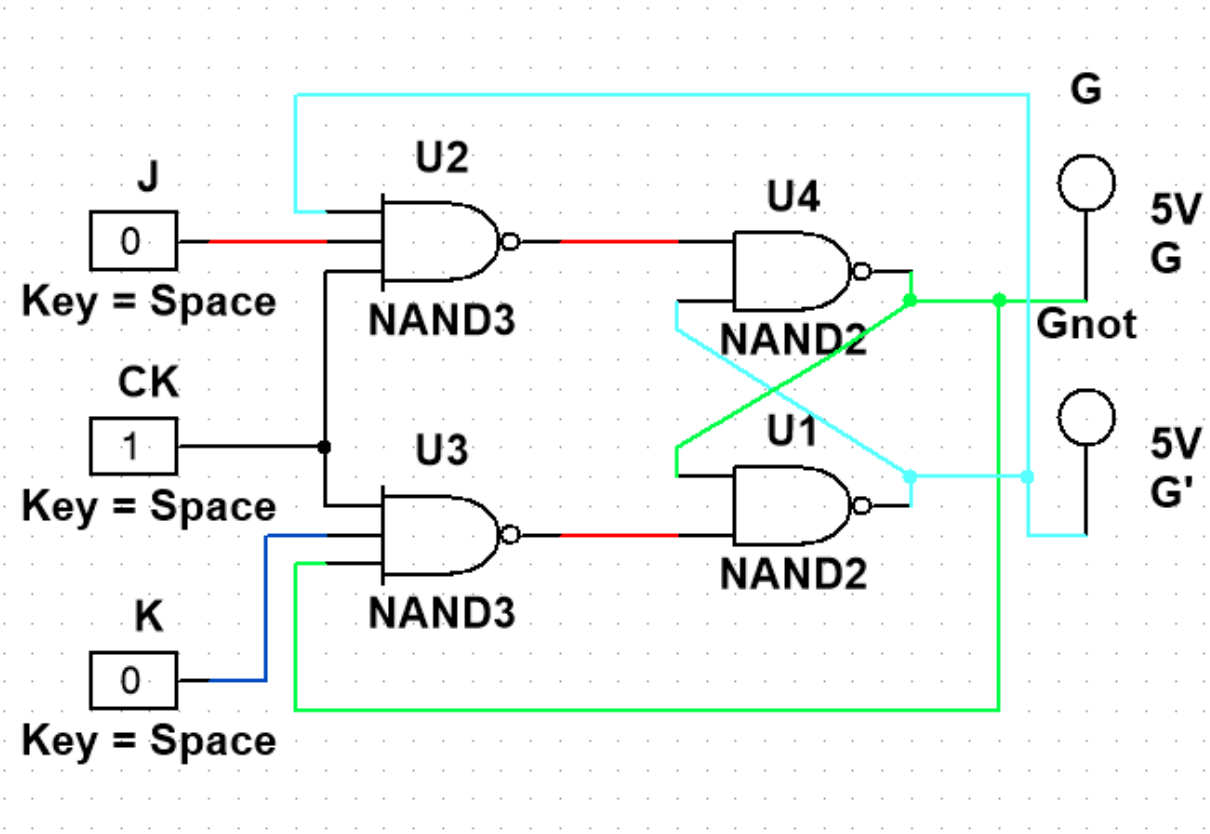

S
A
1
Key = Space
XORAA
2.5V
Sum (S)
74LS86N
C2
B
0
Key = Space
ANDAA
2.5V
Carry-Out (C-Out)
74LS08N


S
A
1
Key = Space
XORAA
2.5V
Sum (S)
74LS86N
C2
B
1
Key = Space
ANDAA
2.5V
Carry-Out (C-Out)
74LS08N

Truth Table

| A | B | D | B0 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

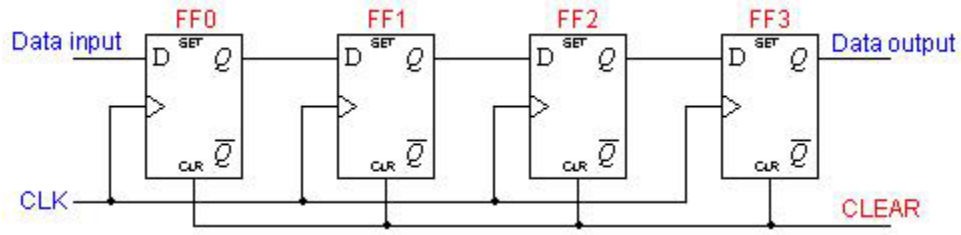
**(c) J K Flip flop**




Truth Table

| CK | J | K | Q | Q |
|---|---|---|---|---|
| 1 | 0 | 0 | - | - |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

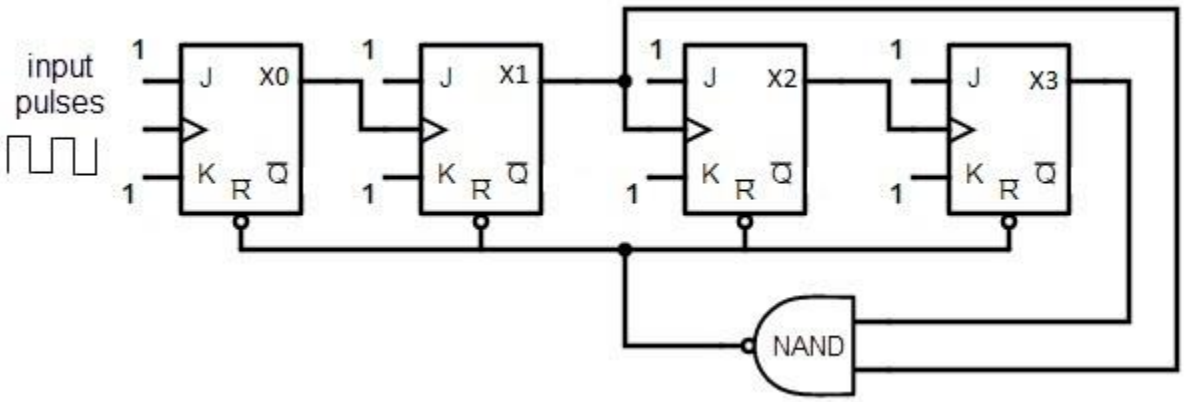
**(d) Serial in-serial Out shift register**




Truth Table:

| Clock Pulse No | QA | QB | QC | QD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 | 0 |

**(E)Synchronous BCD Counter**




## Truth Table of Decade Counter

| Input Pulses | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 (resets) |