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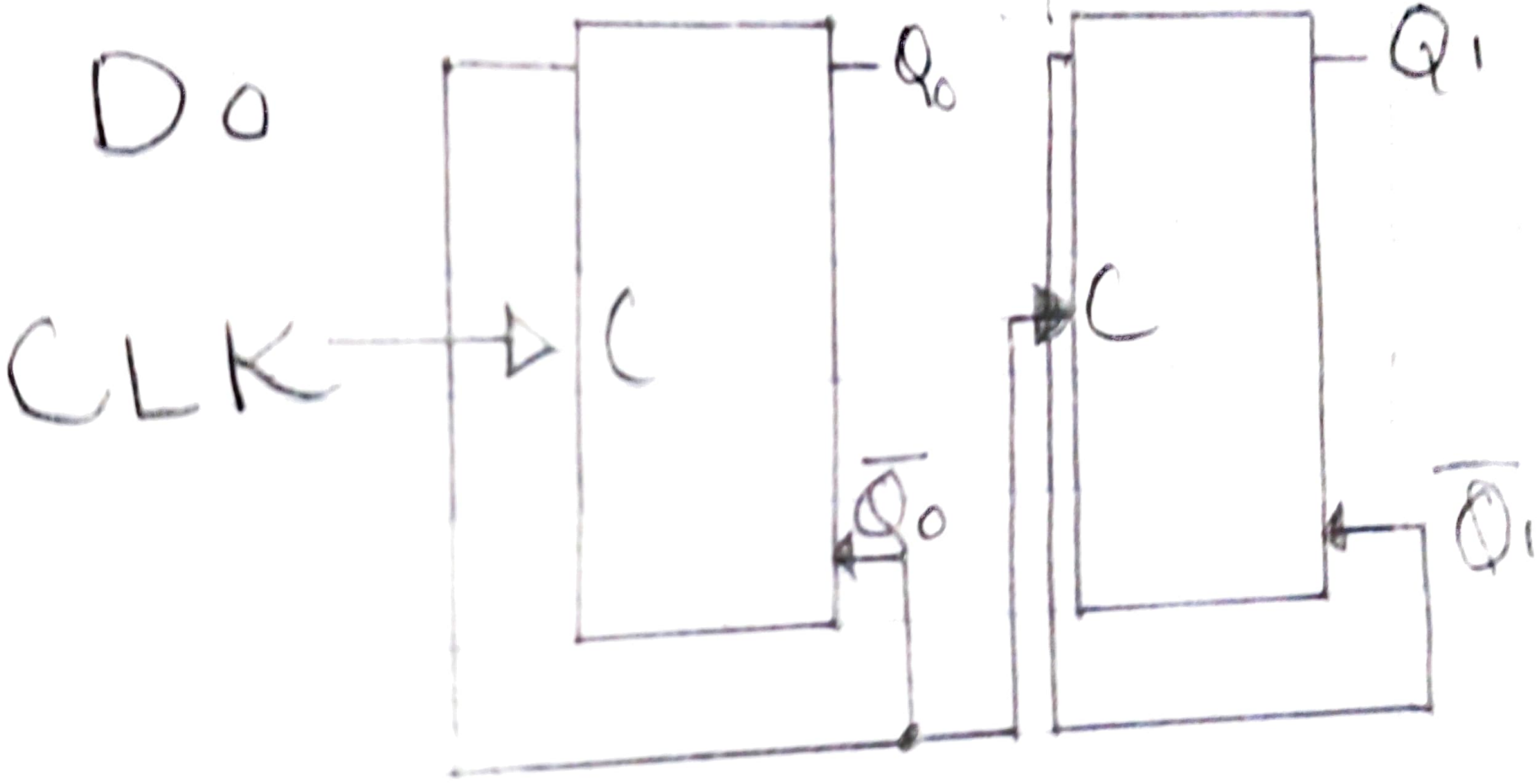
15385

DLD - Assignment #8

Q : 1

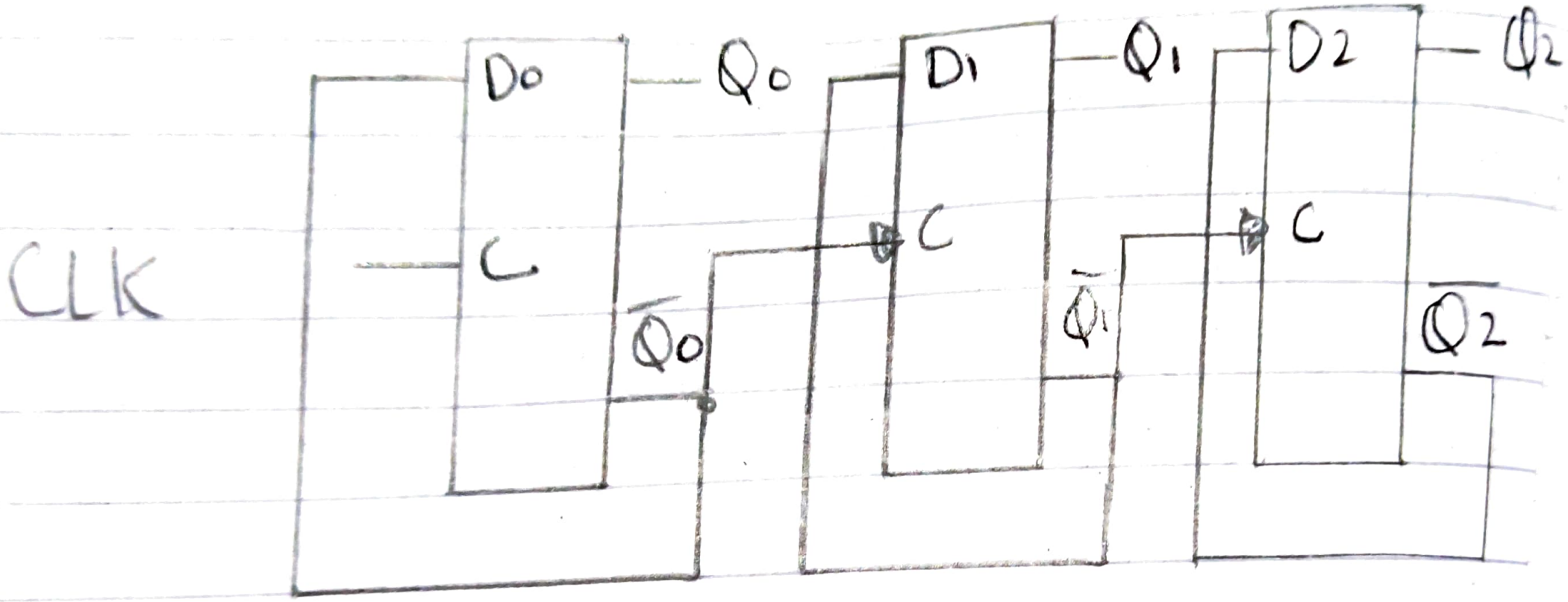


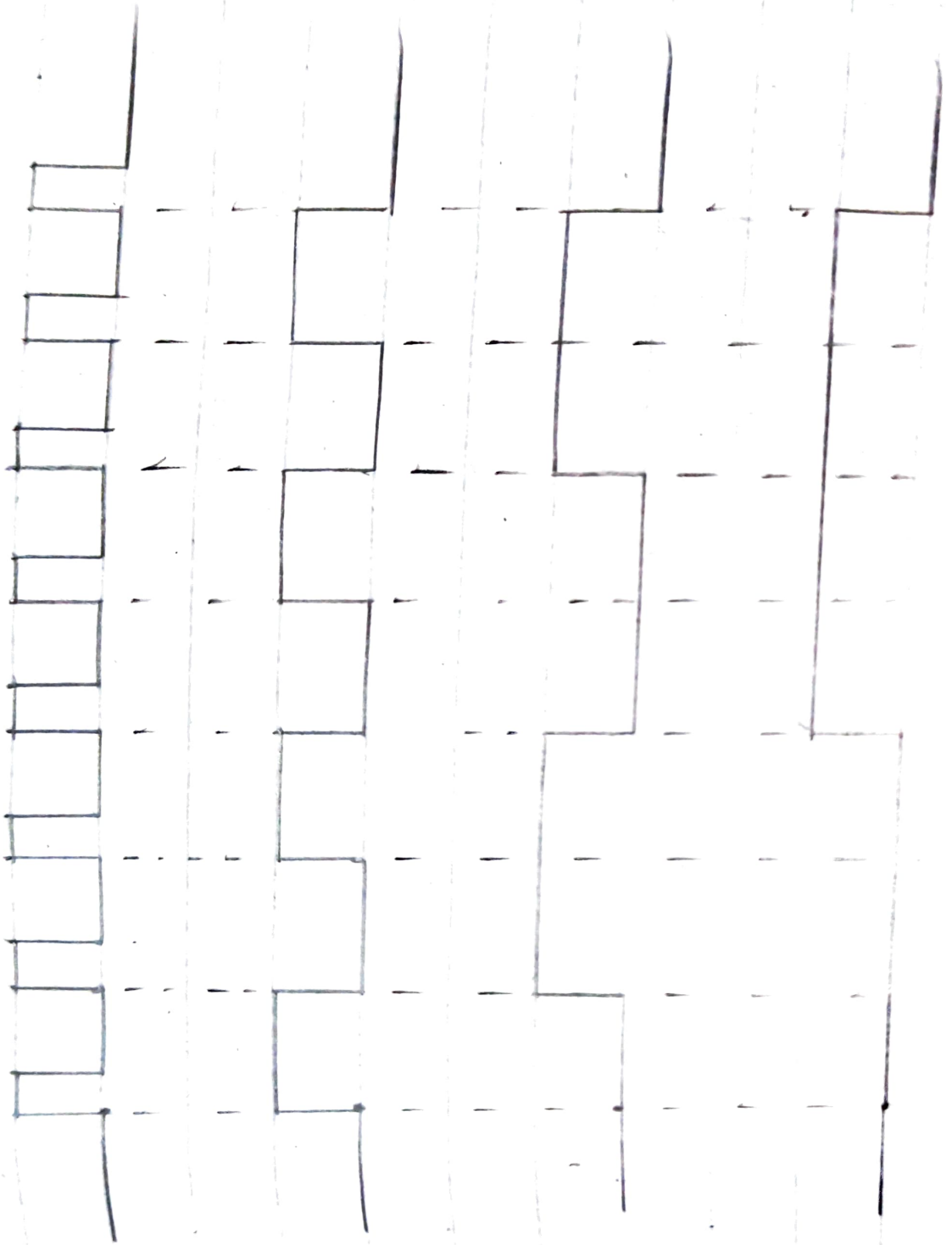
Q
Q0
Q1
CLK

Clock pulse	Q_1	Q_0
initially	0	0
1	0	1
2	1	0
3	1	1
4 (Recycles)	0	0

Q : 2

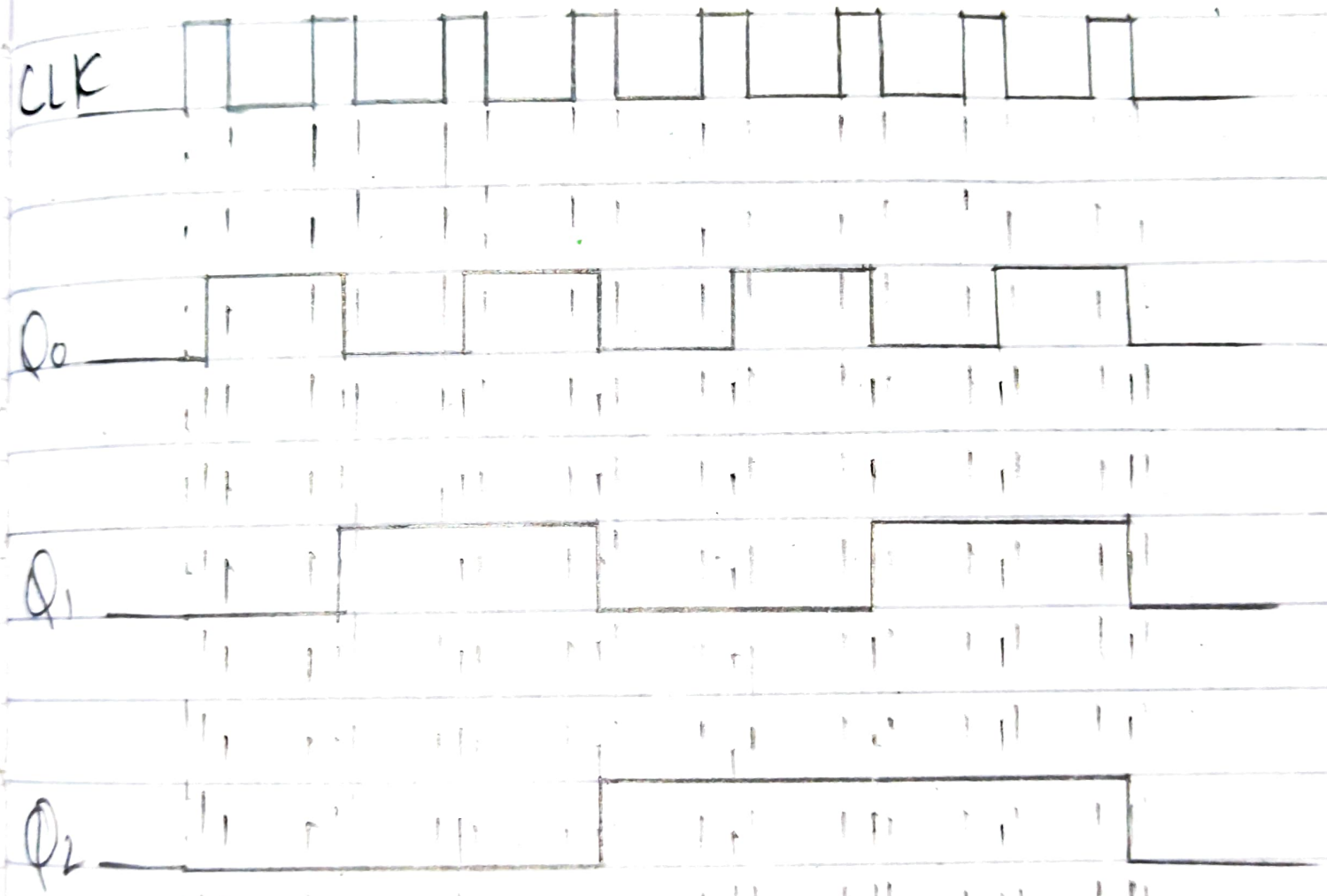
Answer





Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (Recycles)	0	0	0

Q : 3



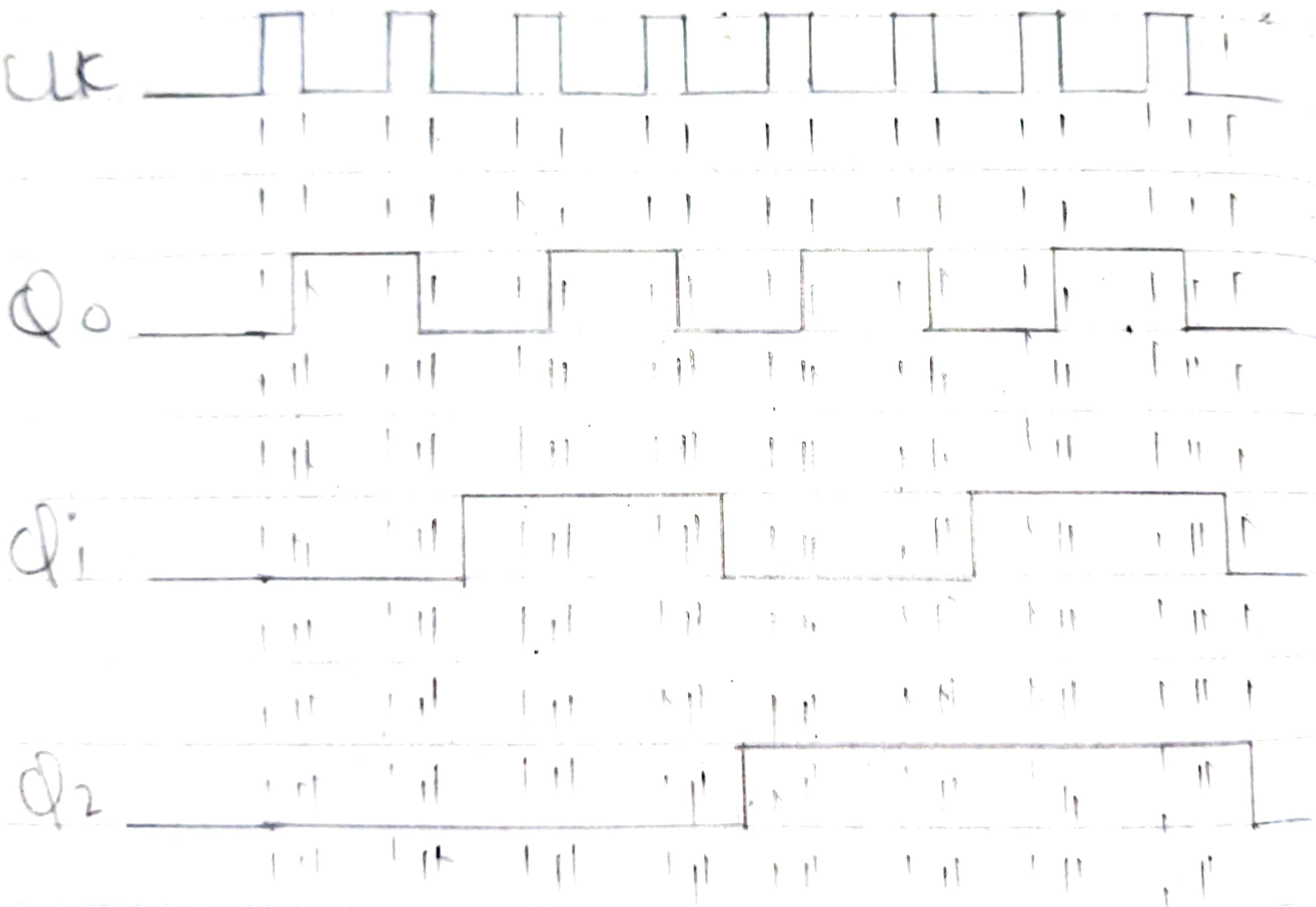
The worst case delay occurs on

clk — Q o

The highest delay is ons, because in the case of synchronous binary counters, the propegation delay is independent of the numbers of flip-flops used.

Q : 4

Answer
Asynchronous



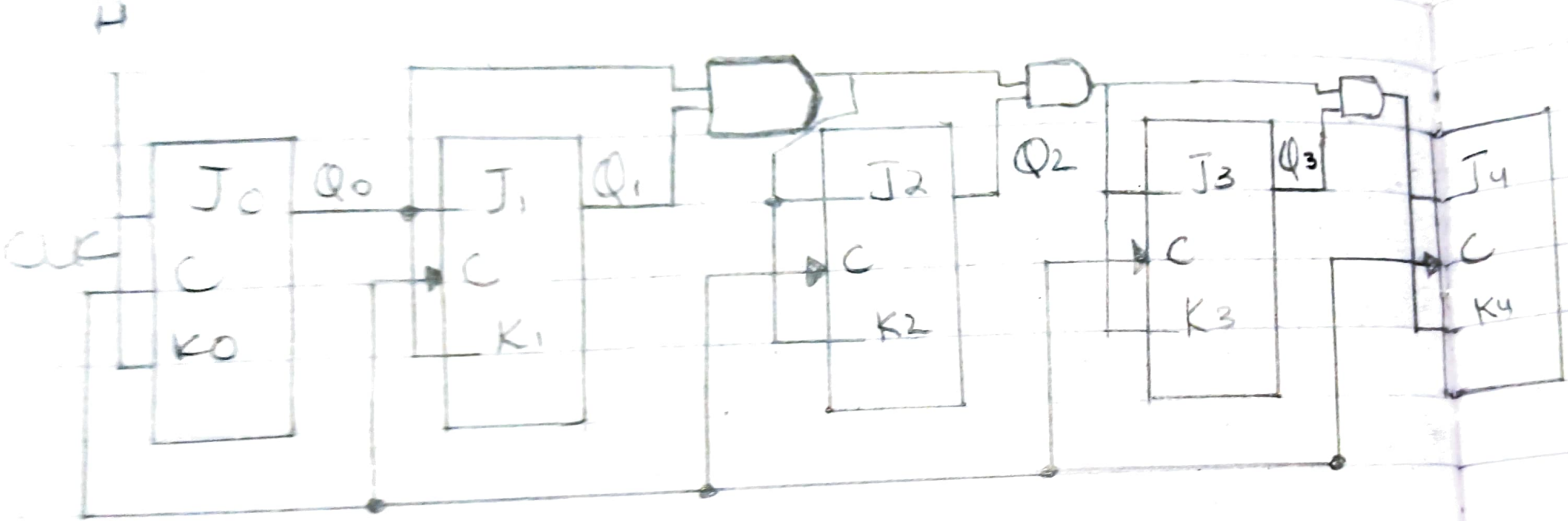
The worst case time occures at Q2.

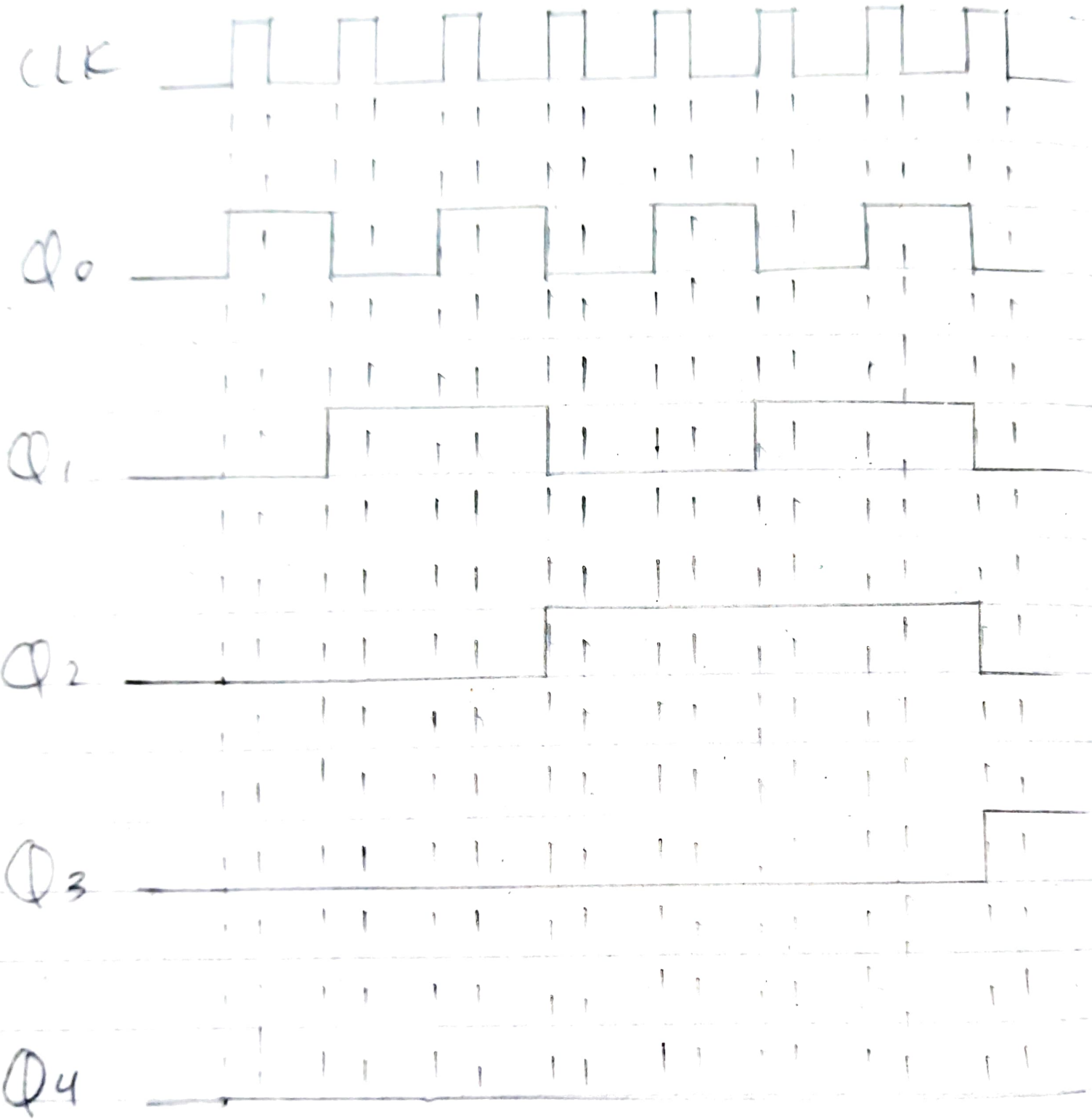
The delay interval timer equals to the delay time at Q2

3 (8ns) = 24ns

Q : 5

Answer.




CLK
Q0
Q1
Q2
Q3
Q4

32	0	0	0	0	0
C.pulse	Q_0	Q_1	Q_2	Q_3	Q_4
Initially	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0

17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0