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ID : 15431

Assignment : no 8

Subject : Digital Logic Design

Course code(CS) : CSC-201

Program : BC (CS)

Assignment No : 8

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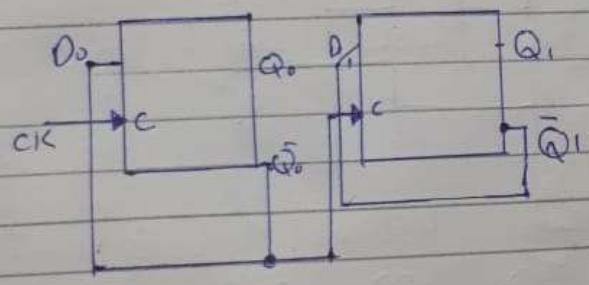
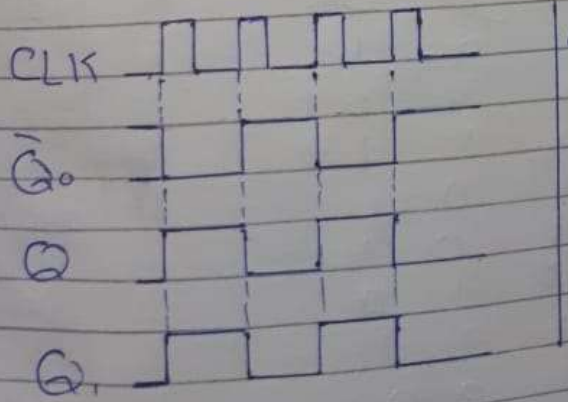
Subject : DLD

Program : BC(CS)

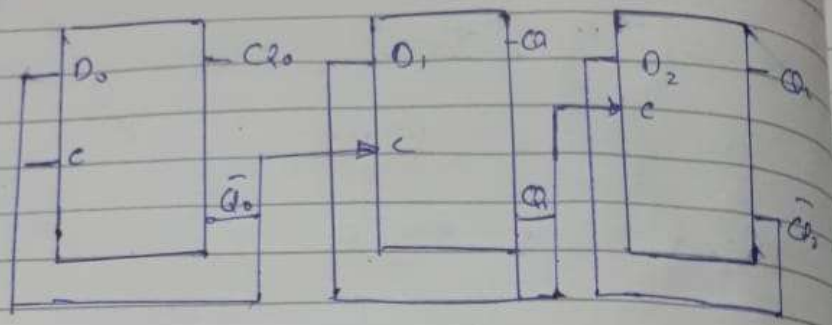
Q1

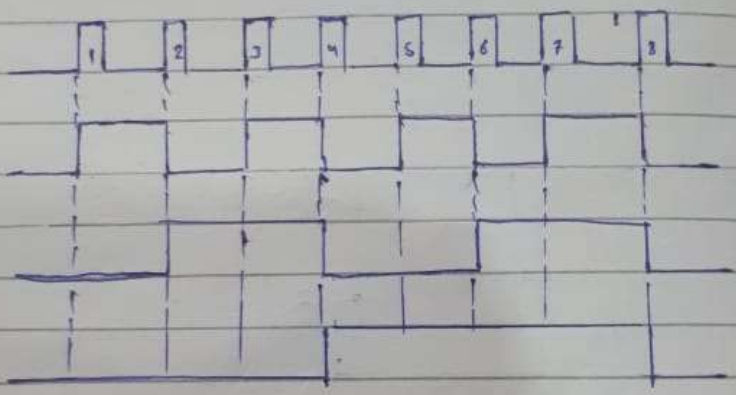




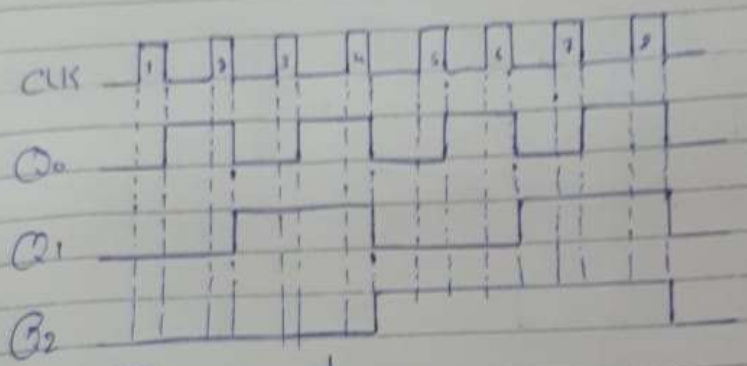
Clock falls	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (Repeats)	0	0

Q.2





C Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (Recycle)	0	0	0

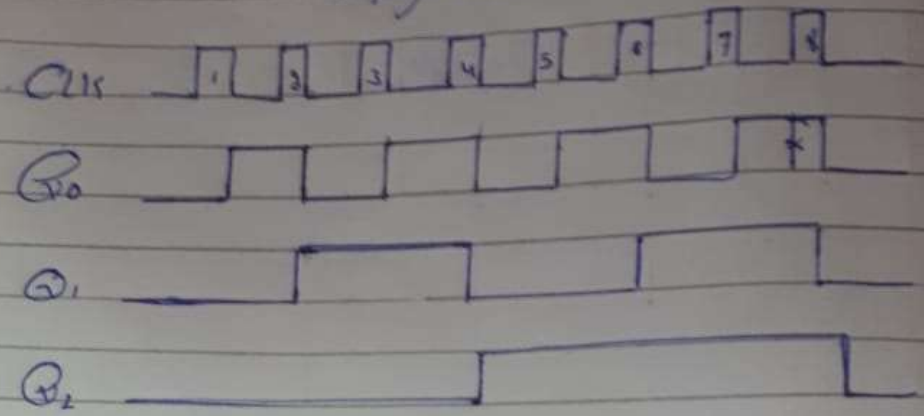


The worst case delay occurs on CLK - Q0.

The highest delay is 8ns because in the case of synchronous binary counter the propagation delay is independent of the number of flip-flops used.

Q4:

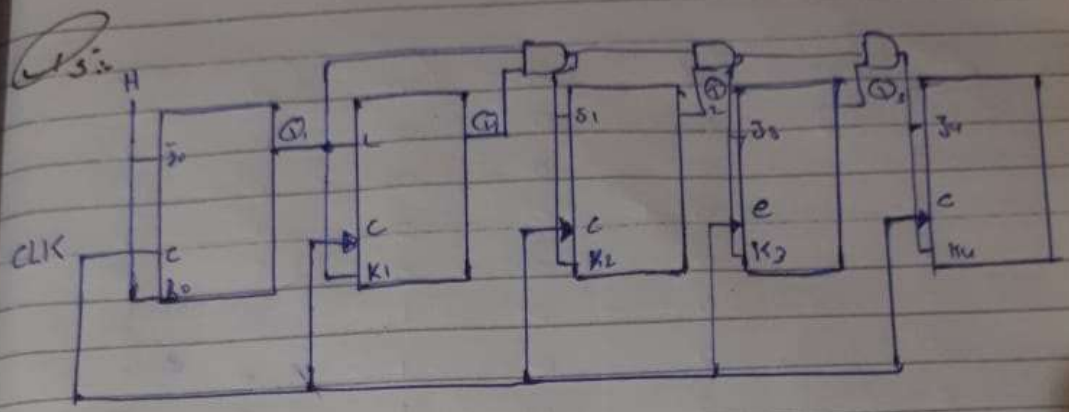
Asynchronous



The worst case delay time occurs at Q2.

The delay interval equals to four time the delay time at Q2.

3 (8ns) = 24ns


H
CLK
C
C
C
e


CLK
1
2
3
4
5
6
7
8

C. Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
Initially	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1