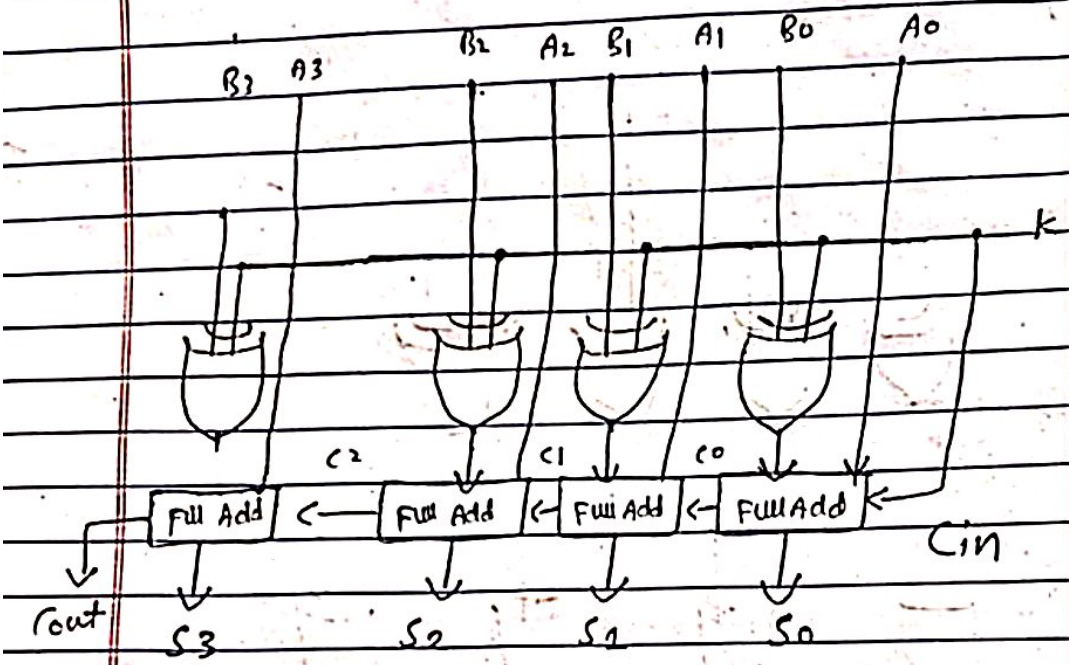
Question 1:

part A :-

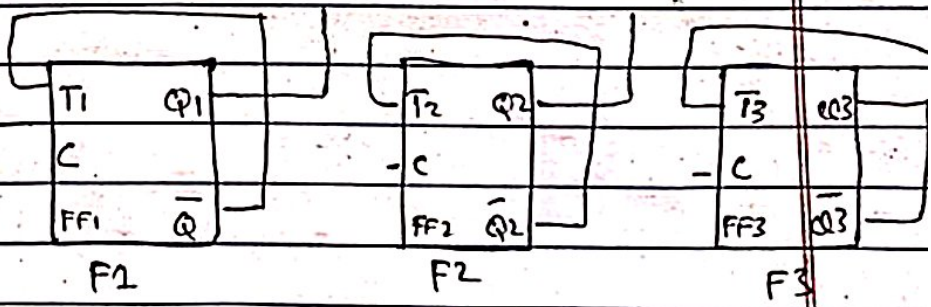



In Digital Circuits, A Binary adder-subtractor is one which is capable of both addition and subtraction of Binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of ALU (Arethmatic logic unit) This circuit requires prerequisite knowledge of XOR Gate, Binary addition and subtraction, full adders the circuit consists of 4 full adders since

we are performing operation on 4 bit numbers. There is a control line Ic that holds a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction.
For an n bit binary adder-Subtractor we use n number of full adderss.

Question 2", part (d)

Frequency divide (use 3J-K Flip Flop and assure 16 KHz frequency as initial wave form.



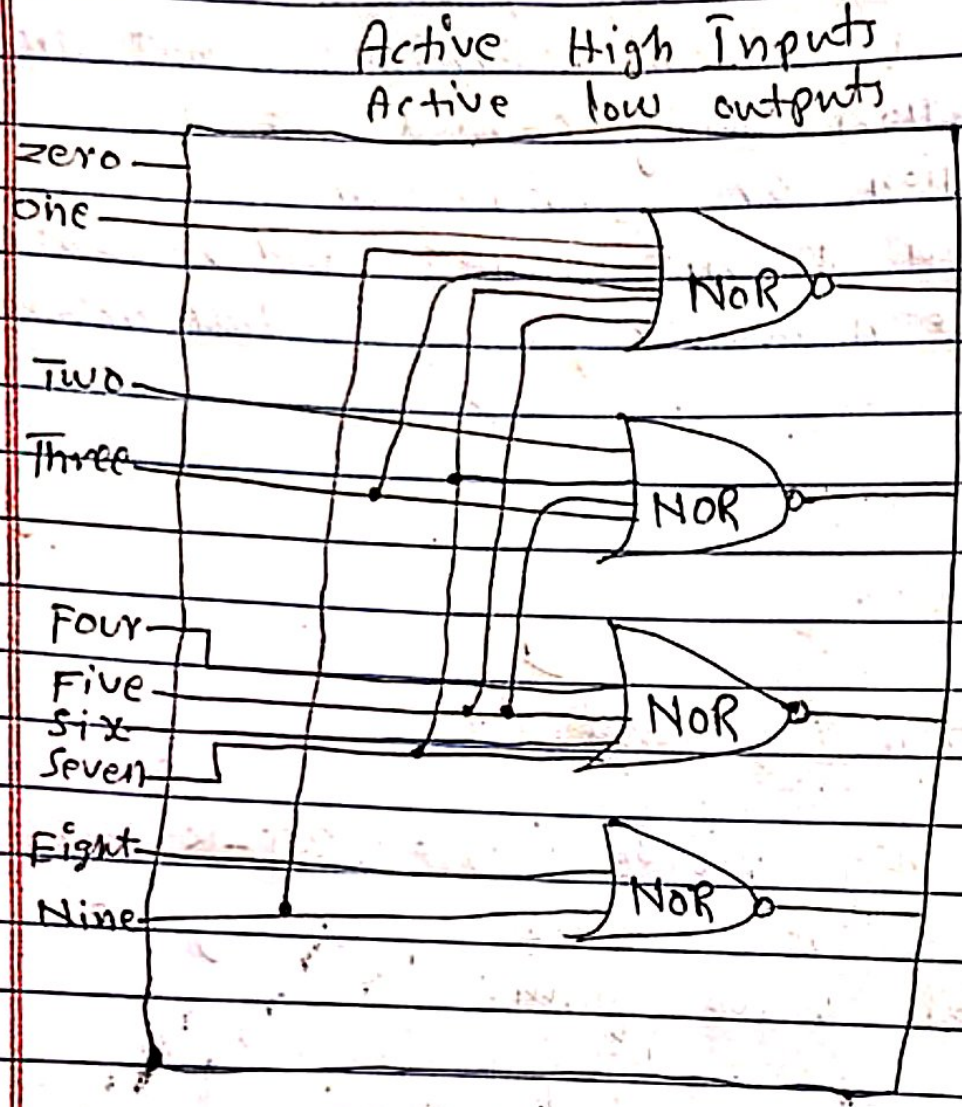

Here we assume the frequency is 16 KHz

so f 12, F = 16/2

F = 8 KHz.

Question 1 :-

point (




b

A simple decimal to BCD encodes is a digital circuit that has 10 input lines and 4 out lines. The inputs represents the 10 decimal numbers from 0 to 9, where only one input can be active. the output indicates the BCD code that represent active input.

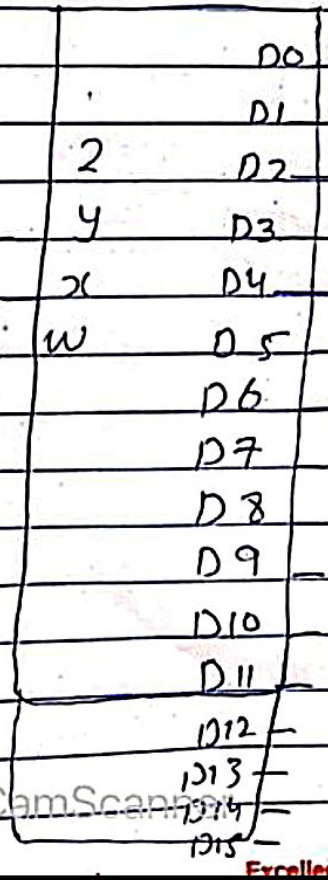
Question 1 part (B)

4 bit active low decoder

A decoder is a building block that takes in an n-bit binary numbers as input.

→ Decodes that binary numbers as input the corresponding output.

→ individual output for every input combination i-e 2nd output






Excellent Good BABAR

Question 2 :- Answer.

| Select data input | | output |
|---|---|---|
| $S_1$ | $S_0$ | Y |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

if $S_1 = 0$ $S_0 = 1$ then $Y = D_0$

Then $Y = D0^{-} (S1) (S0)$

if $S_1 = 1$ and $S_0 = 0$ they $Y = D_1$

then $Y = D_1 (S_1) S_0^{-}$

if $S_1 = 1$ and $S_0 = 1$ then $Y = D_2$

then $Y = D\bar{2}\ S_1 (S_0)$

if $S_1 = 0$ and $S_0 = 0$ the $Y = D_3$

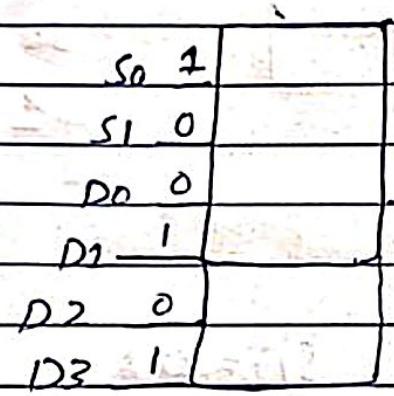
then $Y = D_3\ S_1^{-}\ S_0^{-}$

$Y = D\bar{0} (S_1)^{-} (S_0) - O_1 (S_1) S\bar{0} - D2$
$S_1 (S_0) - D S_1 - S_0^{-}$

Question

For 4 input multiplexer, data inputs are given as
$D_0 = 0$ $D_1 = 1$ $D_2 = 0$ $D_3 = 1$
Find output x, if select input are

(a) $S_0 = 1$, $S_1 = 0$

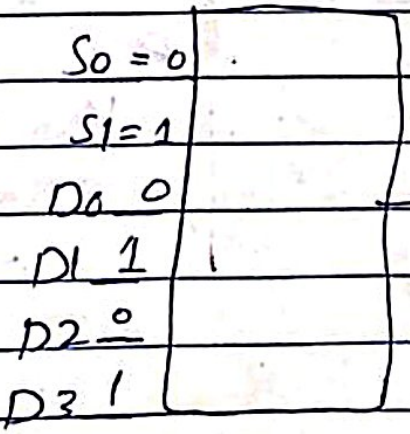



$D_0 = 1$

Y

$S_0 \cdot S_1 = 10 \cdot D_0$

(b) $S_0 = 0$, $S_1 = 1$

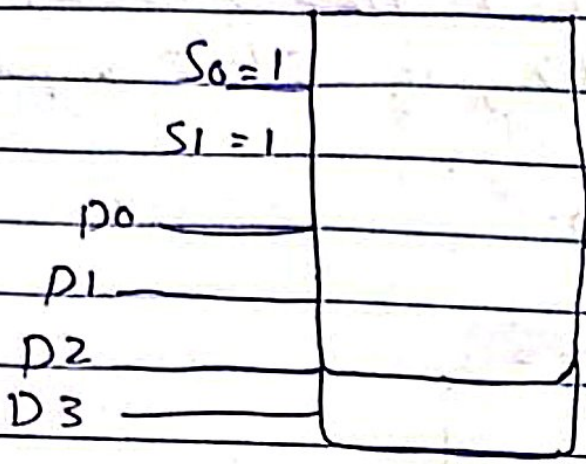



D

$S_0 \cdot S_1 = D_1$

$0 \cdot 1$

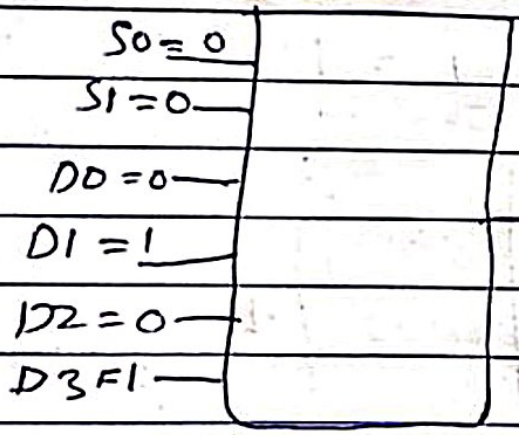
(c) $S_0 = 1, \quad S_1 = 1$




$S_0 \cdot S_1 = D_2$

$1 \cdot 0$

(d) $S_0 = 0, \quad S_1 = 0$

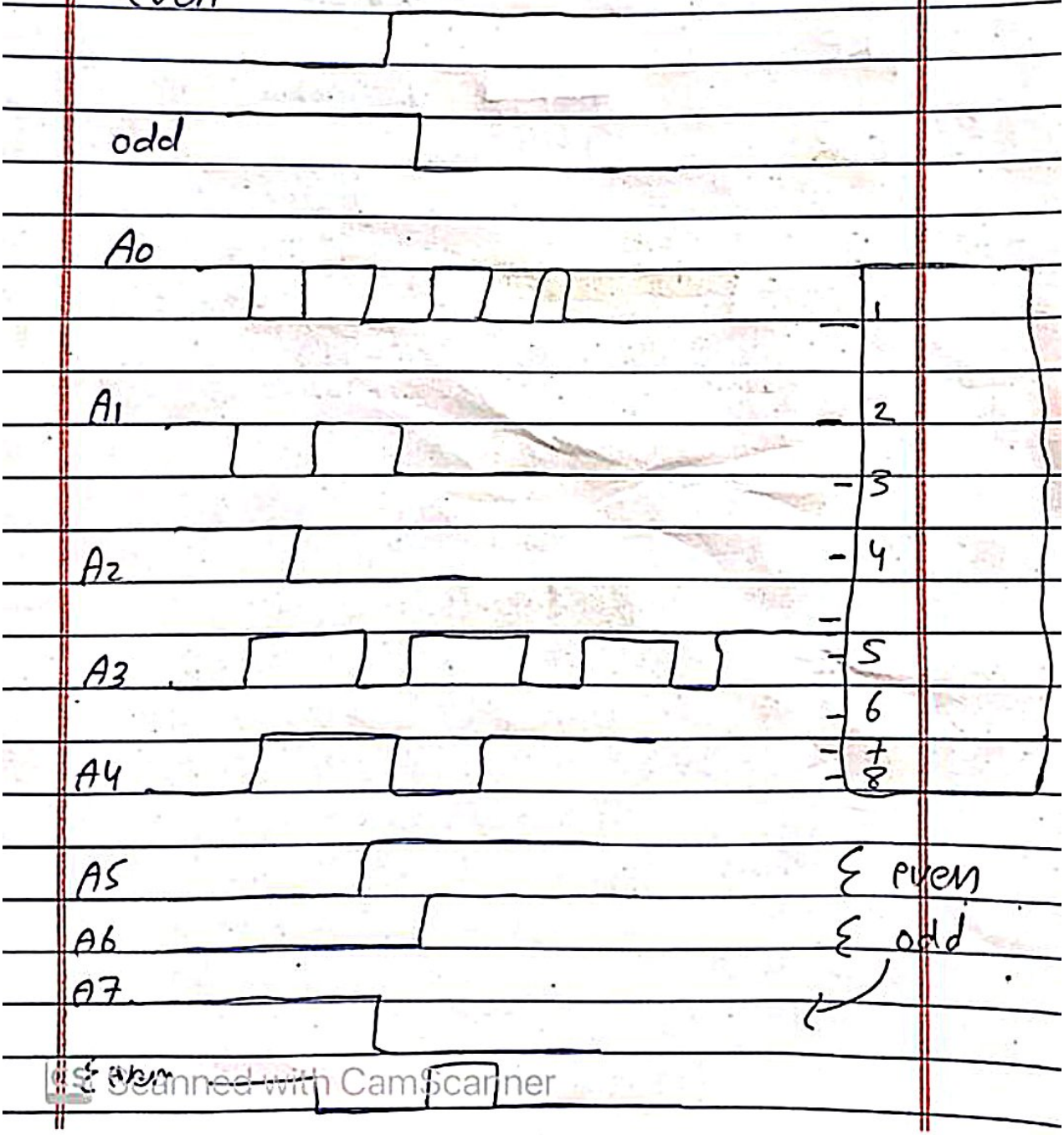



$S_0 \cdot S_1 = D_3$

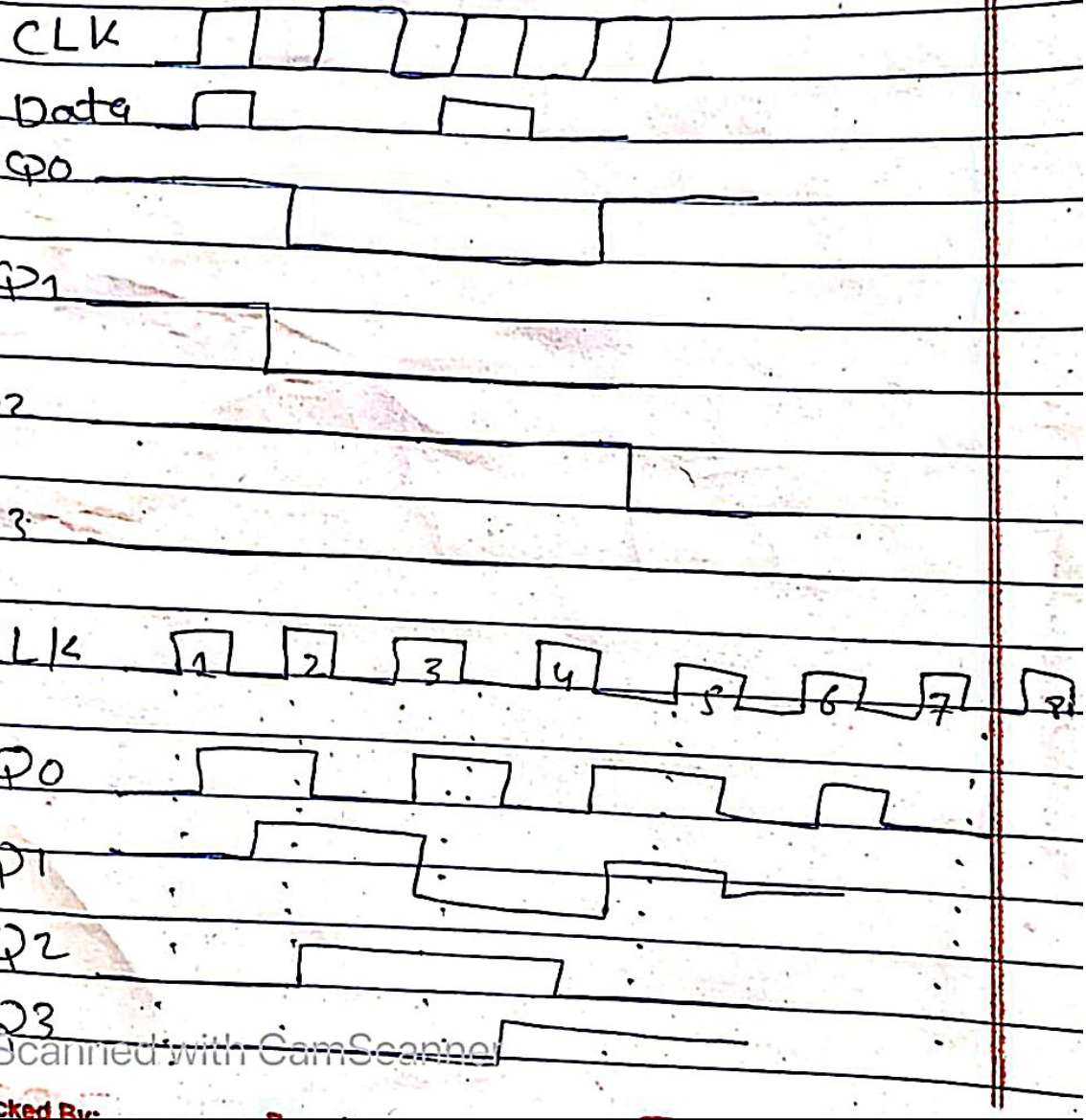
$1 \; 1$

Question 3:-

Timing Diagram in figure 01 shows inputs to a 9 bit parity checker Draw the ξ even and ξ odd, ouput for every parity checker.

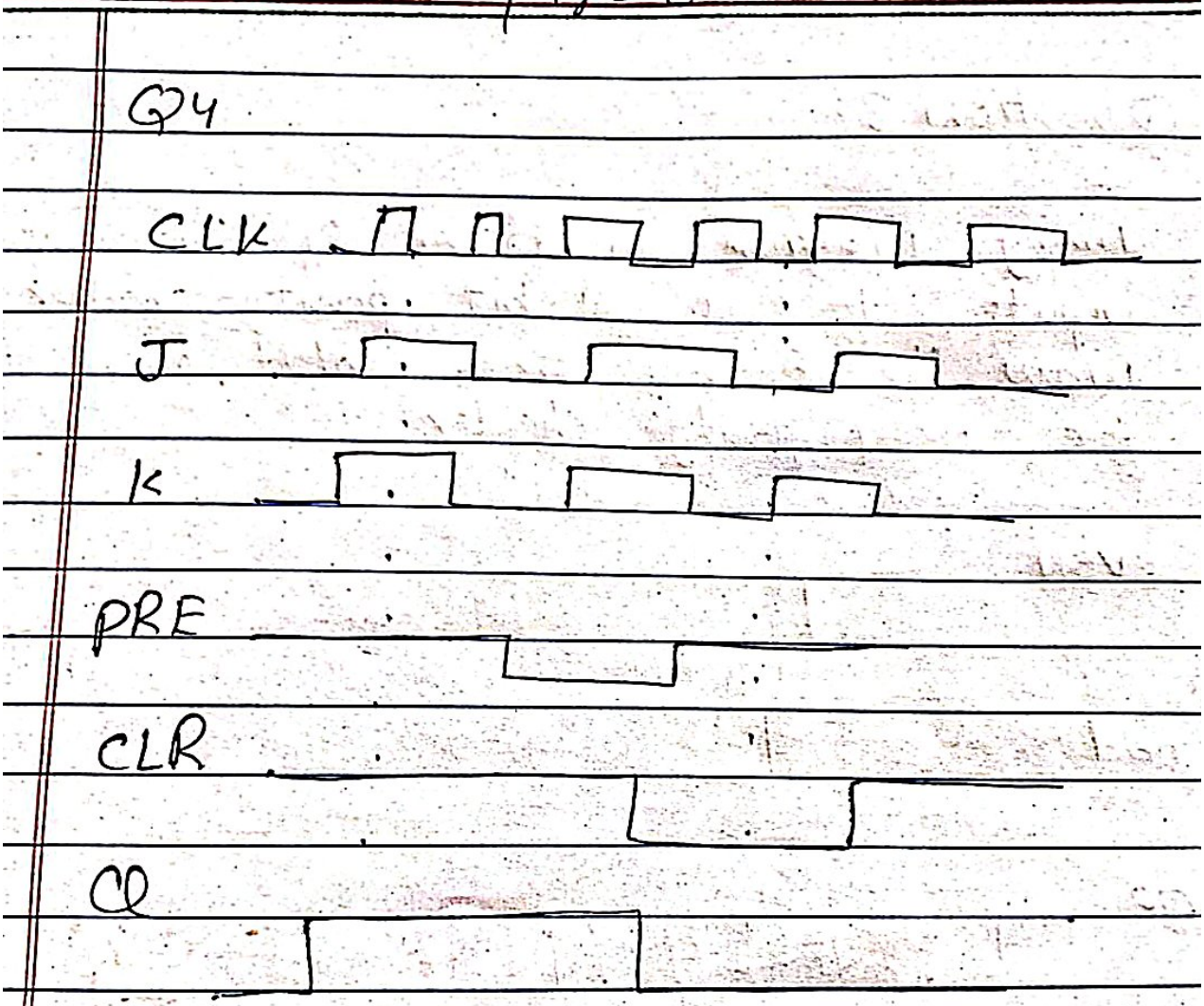


Q5 :-






Checked By:



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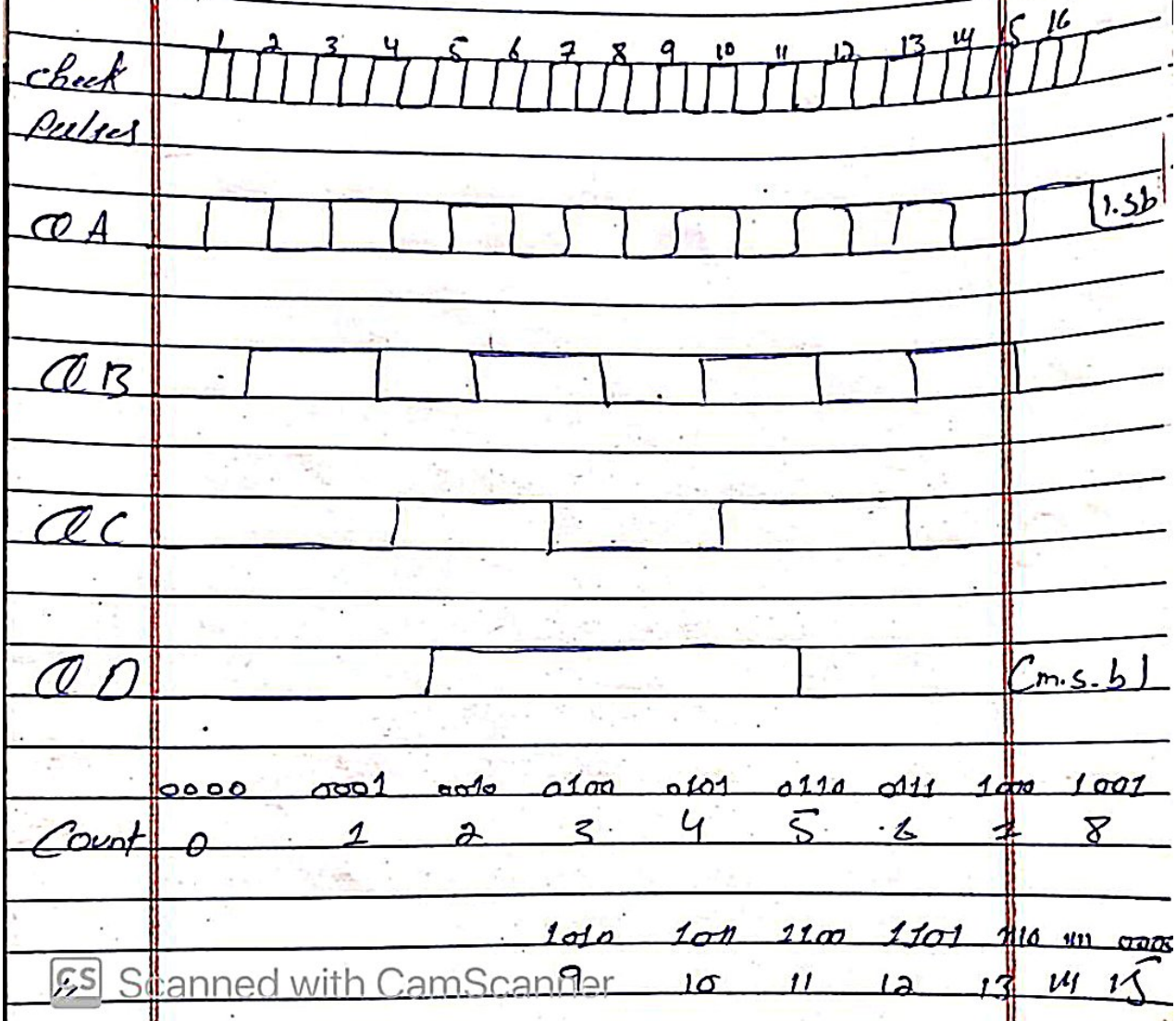
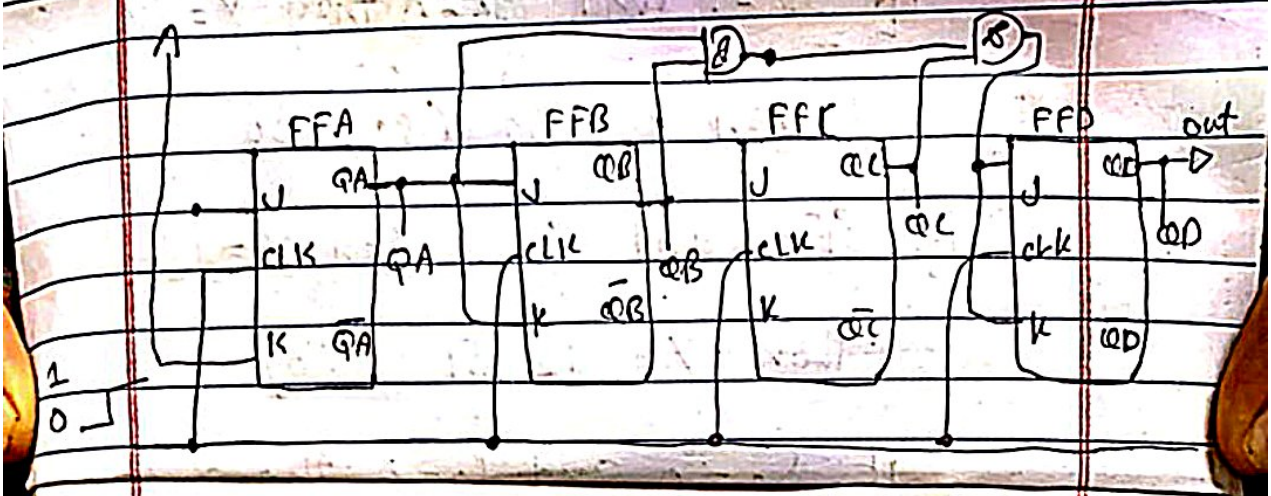
## Question 6

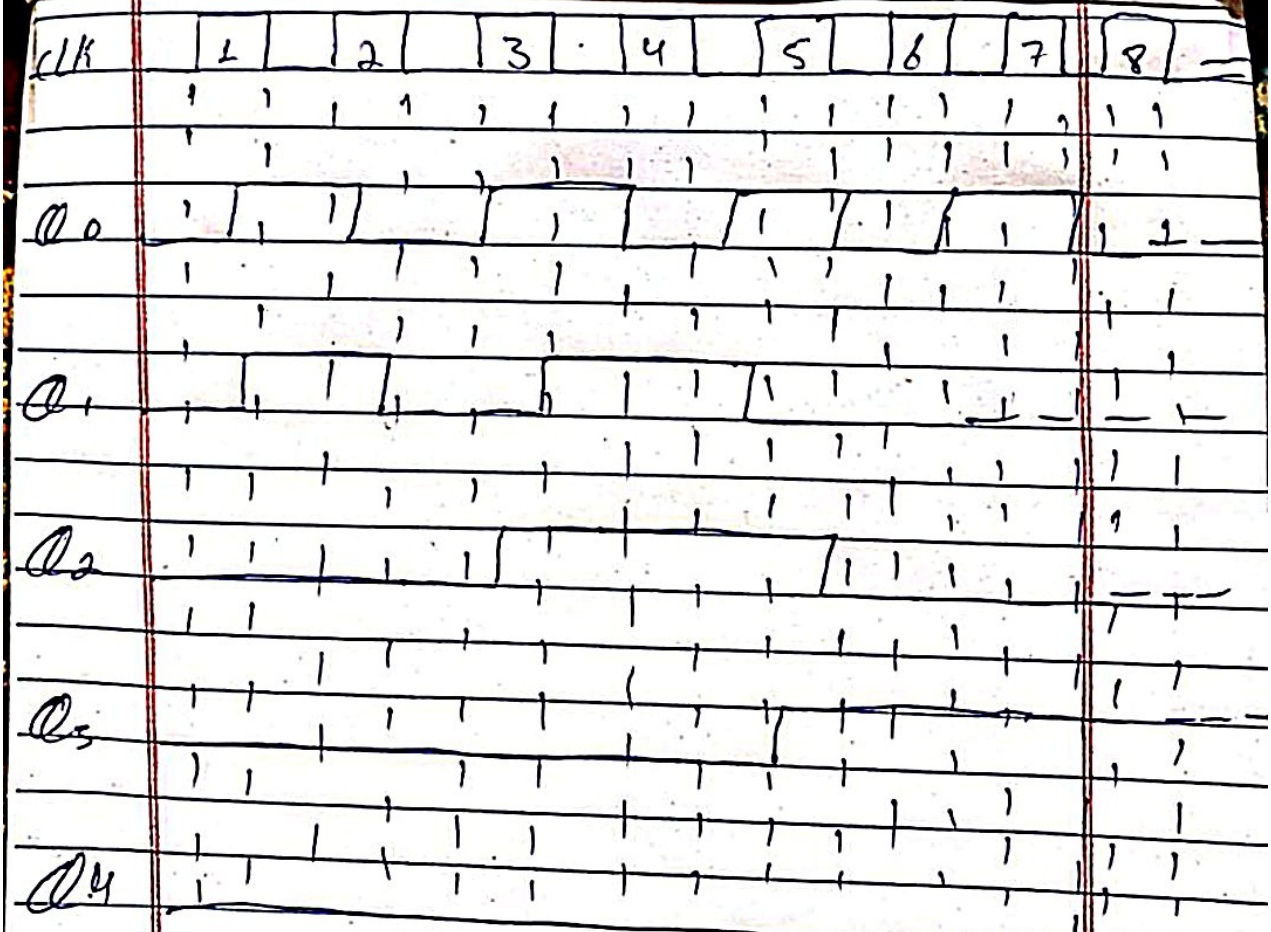



| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 0000 | 0001 | 0010 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 |
| Count | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 1010 | 1011 | 1100 | 1101 | 1110 | 1111 | 0000 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 |

Question 6:- page



Day. M T W T F S

Date:

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