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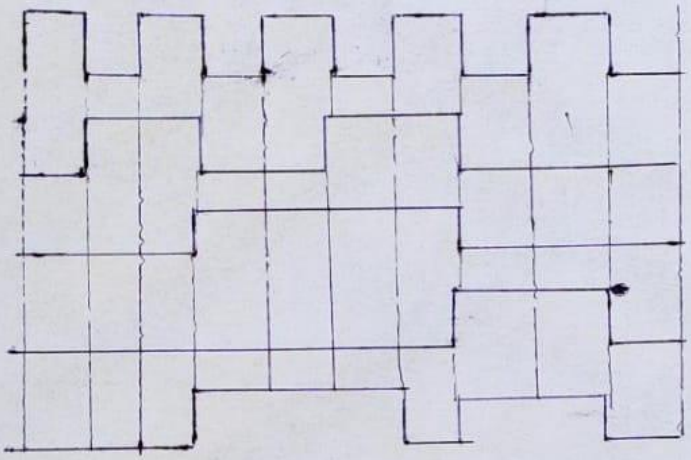
Reg# 16549

Semester: 6th

Final Paper: DIGITAL LOGIC AND DESIGN (THEORY)

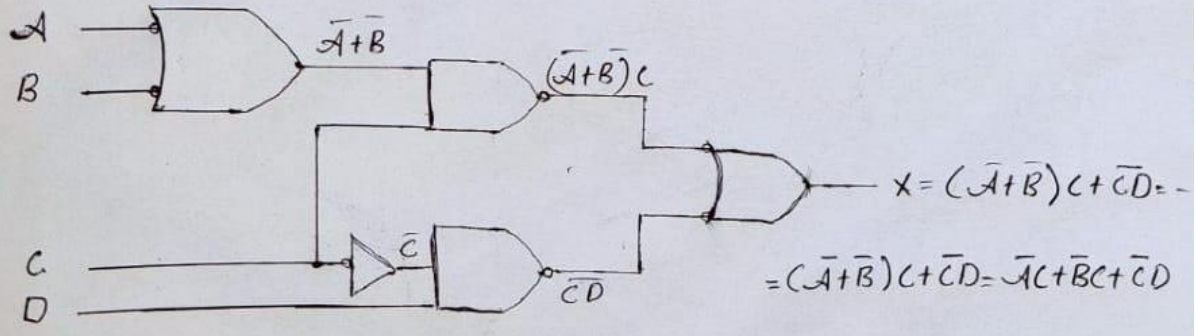
Submitted to: Sir MUHAMMAD AMIN

Q1:- Draw the logic circuit using the input (A, B, C, D) and output (X) waveforms in Figure 01.



Answer:-

Solution.



Q2: For the 4-Input multiplexer, data inputs are given as

$D = 0,\ D_1 = 1,\ D_2 = 0,\ D = 1$

Find the Output Y if the select inputs are given as

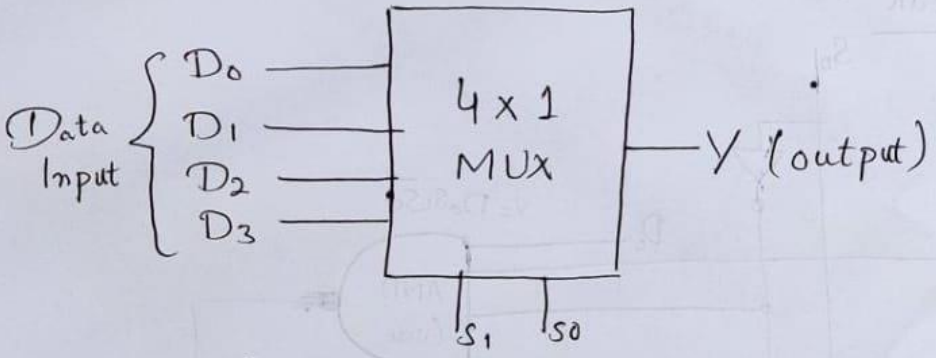
a) $S_0 = 1,\ S_1 = 0$

$S_0 = 0,\ S_1 = 1$

$S_0 = 1,\ S_1 = 1$

$S_0 = 0,\ S_1 = 0$

Answer:



Find Select lines:-

$n = 4$

$m = \log_2 n$

$m = \log_2 4$

$= \log_2 2^2 \quad \because \log_a a = 1$

$m = 2 \log_2 2 \quad 1 = 2 \cdot 1 = 2 \longrightarrow$ Select lines

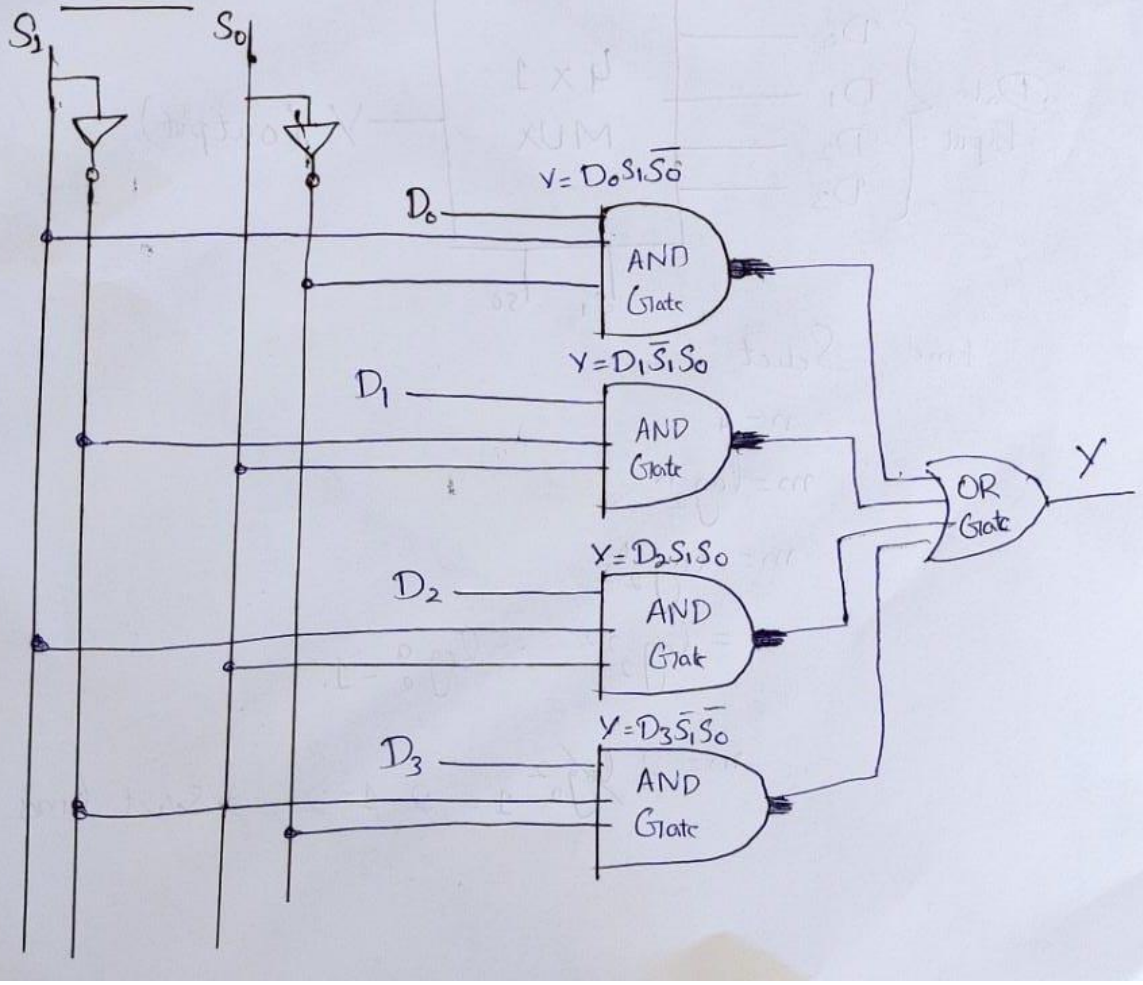
S_0	S_1	Data
1	0	D_0
0	1	D_1
1	1	D_2
0	0	D_3

Output (Y)

$Y = D_0 S_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 S_0 + D_3 \bar{S}_1 \bar{S}_0$

OutPut = $Y = D_0 S_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 S_0 + D_3 \bar{S}_1 \bar{S}_0$

Circuit



Q3. For the Circuit in Figure Q2, assume the inputs are $\overline{Add}/Subt = 1$, A = 1010, & B = 1101. What is the Output

Answer-

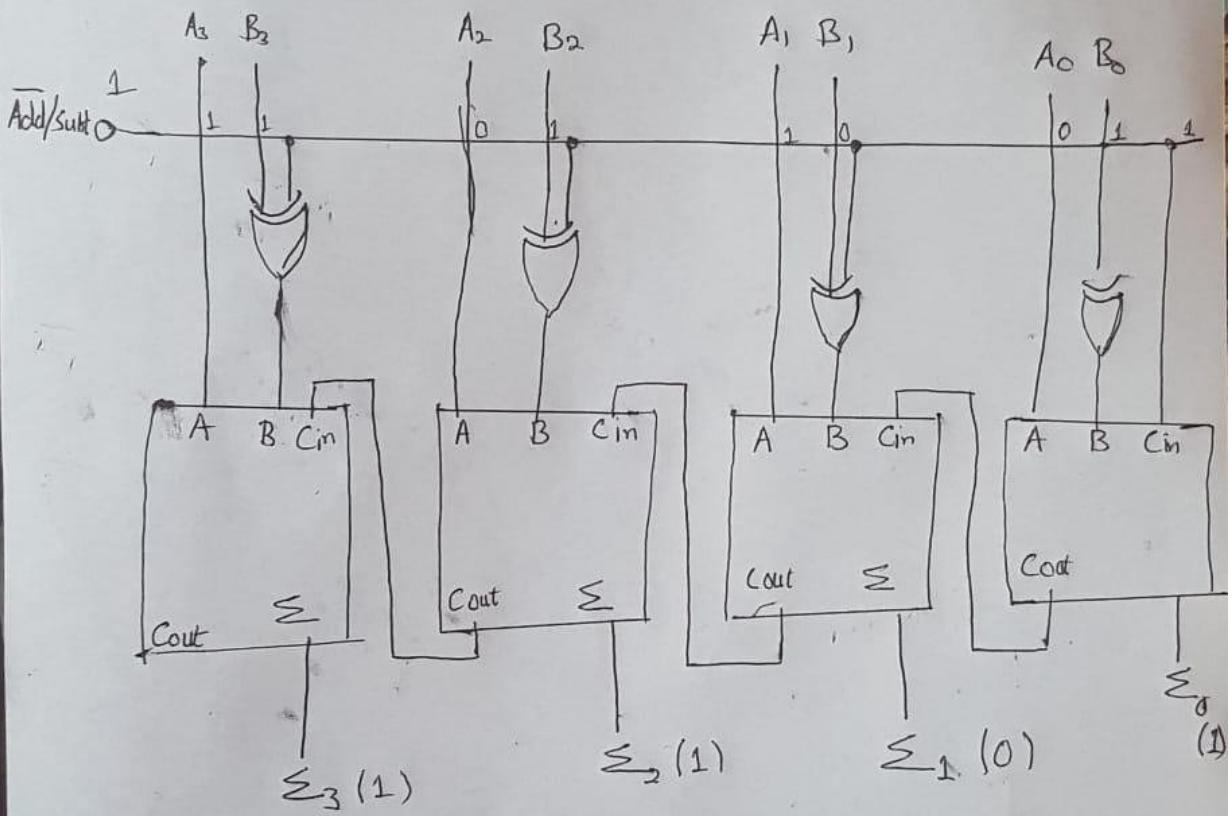
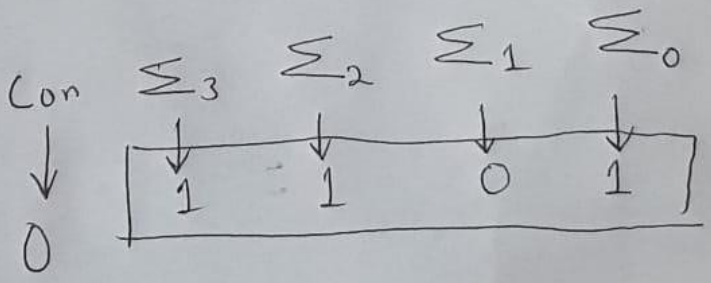


Figure Q2

The Output of the



Q4:- Determine the A = B, A > B, and A < B outputs for the Input numbers shown on the comparator in Figure 03.

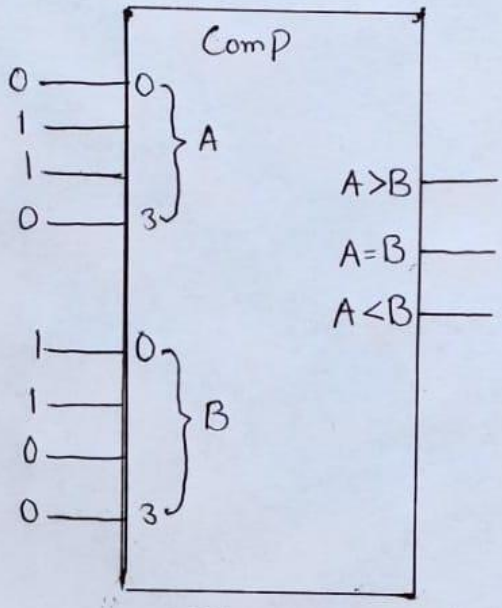


Figure 03

Answer:- The Number on the A Inputs is 0110 and the number on the B inputs is 0011. The A > B output is HIGH and the other outputs are LOW.

Q5:-> show the logic required to convert a 4-bit Gray code to binary and use that logic to convert the following Gray words to binary: 1011.

Answer:-> Solution

convert Gray code to binary code 1011

Method-1: (Gray code to Binary)

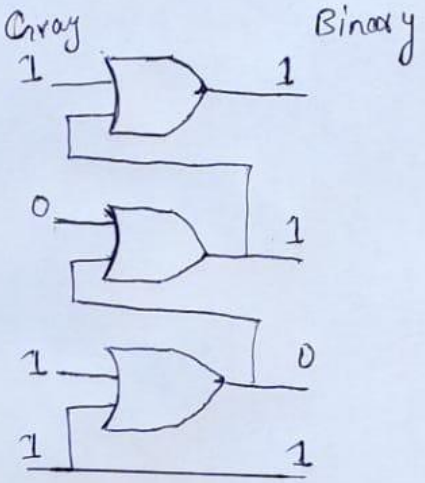
$b_3 = g_3 = 1$

$b_2 = b_2 \oplus g_2 = 1 \oplus 0 = 1$

$b_1 = b_2 \oplus g_1 = 1 \oplus 1 = 0$

$b_0 = b_1 \oplus g_0 = 0 \oplus 1 = 1$

∴ Binary : 1101



Method 2:-> (Gray code to Binary)

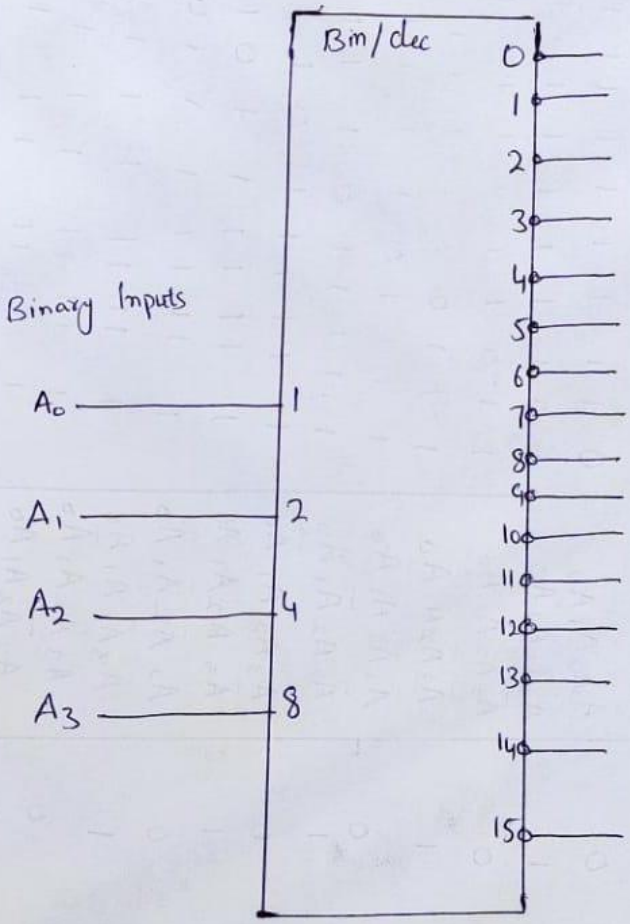
g_3	g_2	g_1	g_0	Gray code
1	0	1	1	
↓	↓	↓	↓	
1 →	1 →	0 →	1	
b_3	b_2	b_1	b_0	
$= g_3$	$= b_3 \oplus g_2$	$= b_2 \oplus g_1$	$= b_1 \oplus g_0$	Binary code.

Binary 1101

Q6:- Draw a circuit of 4-bit active low decoder

4- bit Decoder for Active low

Binary Inputs A_0, A_1, A_2, A_3

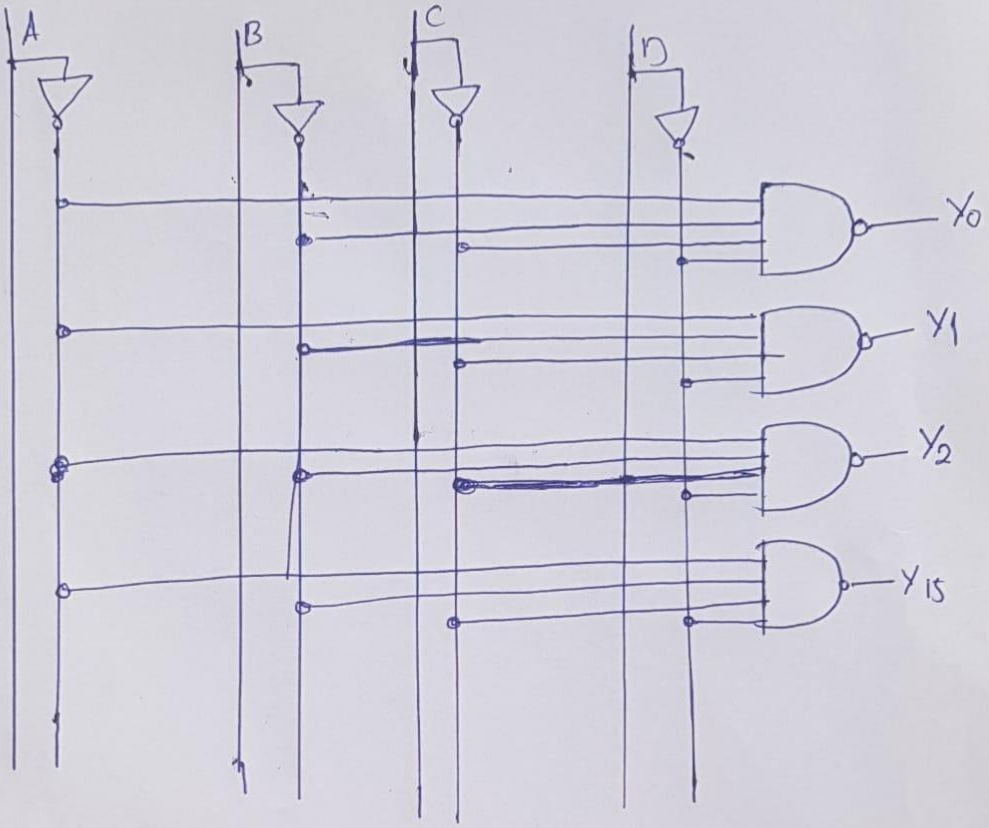


In an ~~acto~~ active - Low output is required for each decoded number, the entire decoder can be implemented with NAND gates & inverters.

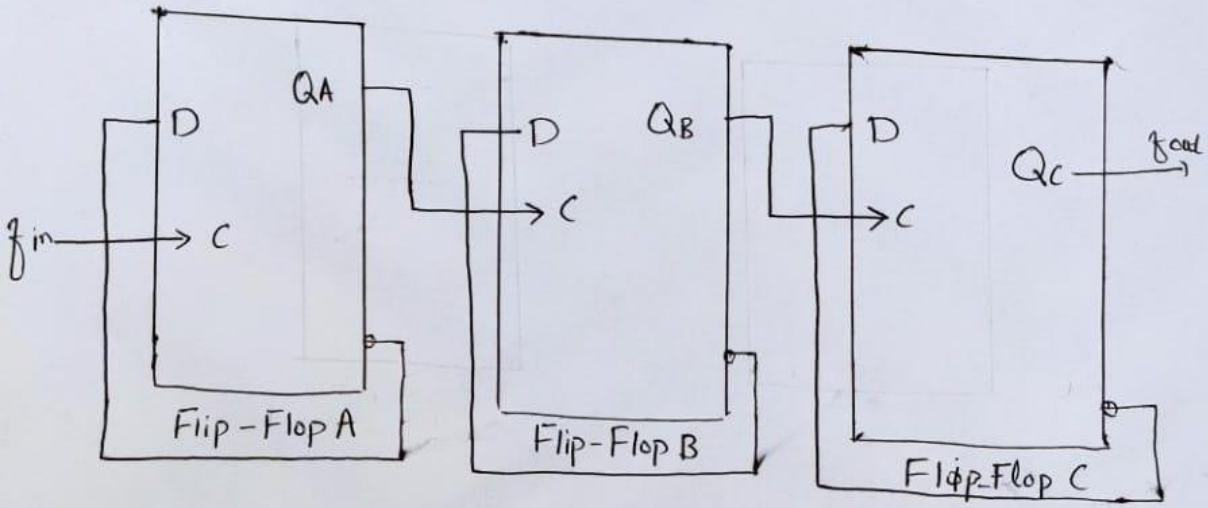
Decoding functions & truth table for 4-bit active-Low decoder Outputs

Decimal Digit	Binary Inputs A_3	A_2	A_1	A_0	Decoding Function	Outputs 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\bar{A}_3\bar{A}_2\bar{A}_1 A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\bar{A}_3\bar{A}_2 A_1\bar{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\bar{A}_3\bar{A}_2 A_1 A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\bar{A}_3 A_2\bar{A}_1\bar{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\bar{A}_3 A_2\bar{A}_1 A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\bar{A}_3 A_2 A_1\bar{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\bar{A}_3 A_2 A_1 A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\bar{A}_2\bar{A}_1 A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\bar{A}_2 A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\bar{A}_2 A_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3 A_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3 A_2\bar{A}_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3 A_2 A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3 A_2 A_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Q6:- Circuit of 4-bit active low

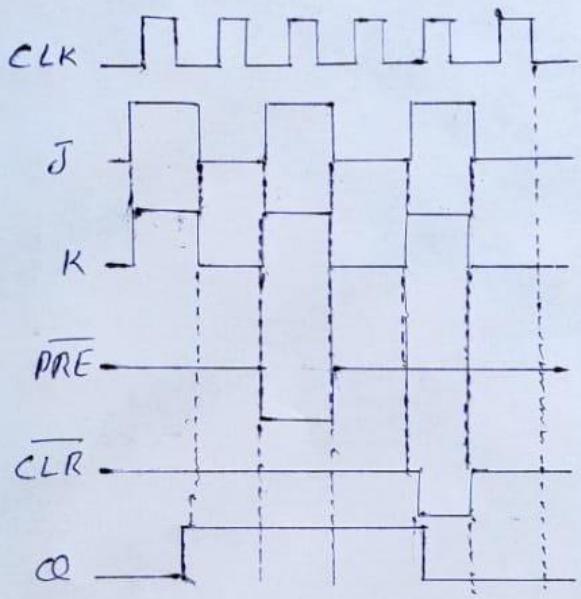


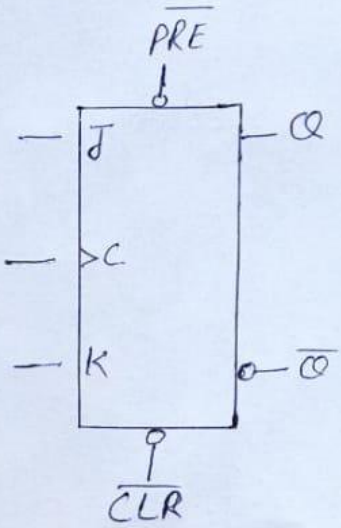
Q7: Frequency divider (Use 3-JK flip flop & assum 16 KHZ frequency of the intial wave form)



Q8:- Determine the Q waveform relative to the clock if the signals shown in Figure 04 are applied to the ~~Outpu~~ Inputs of the J-K flip-flop. Assume that Q is initially Low.

Ans:-

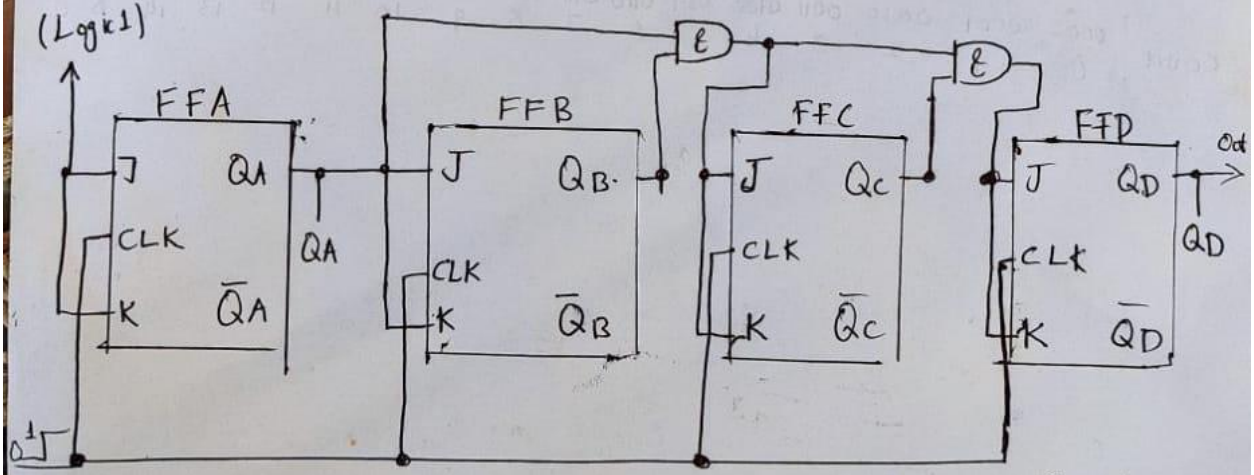




Q9:-

Q:- Draw the logic diagram & timing diagram for the 4-bit stage Synchronous binary Counter. Verify that the waveforms of the Q outputs represent the Proper binary number after each clock pulse.

Ans:- Logic Diagram of 4 Stage Synchronous



4-Stage Synchronous binary Counter

4- Stag Synchronous Counter Wavefom Timing Diagram