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Q.1 Design and verify the logic circuit for the following.

(a) Half adder using logic gates

HALF ADDER

AIM:

Design and verify the logic circuit of Half adder using logic gates .

OBJECTIVES

: • To understand the principle of binary addition. • To understand half adder concept. • Use truth table and Boolean Algebra theorems in simplifying a circuit design. • To implement half adder circuit using logic gates

PROCEDURE:

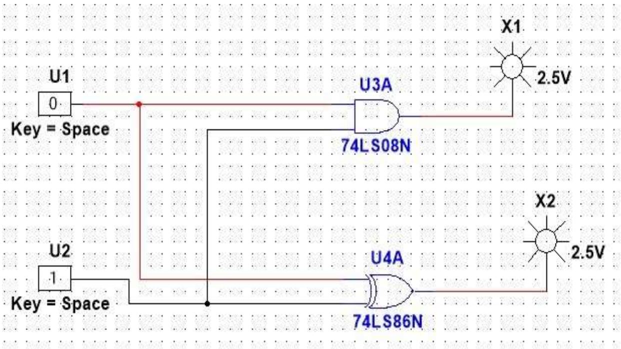
1. collect the components necessary to accomplish this experiment.
2. Plug the IC chip into the breadboard.
3. Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V.
4. According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
5. Connect the inputs of the gate to the input switches of the LED.
6. Connect the output of the gate to the output LEDs.
7. Once all connections have been done, turn on the power switch of the bread-board
8. Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs. HALF ADDER: Half Adder: A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.

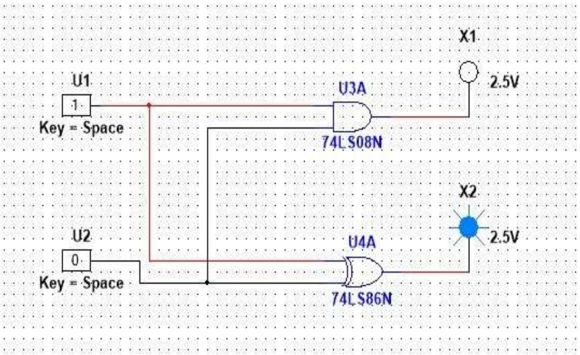
HALF ADDER:

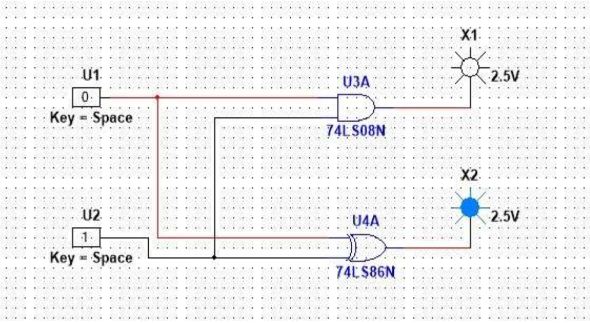
Half Addder: A half adder is a logical circuit that performs an addition operation on,two binary digits. The half a d der produces a sum and a carry value which are both binary digits.

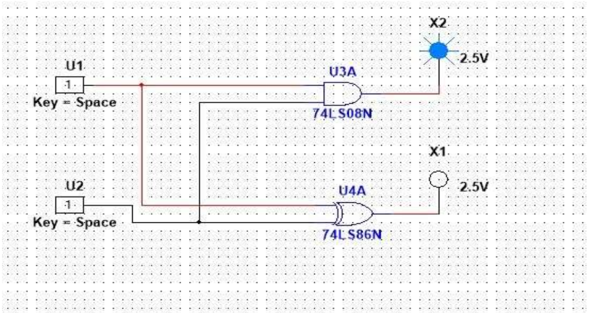
OBSERVATION TABLE.

Inputs		Outputs	
A	B	Sum(S)	Carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1









RESULTS AND ANALYSIS:

Half Adder: Verified the truth table of Half Adder as S = 1 i.e. LED which is connected to S terminal glows when inputs are A, B Verified the truth table of Half-Adder as C = 1 i.e. LED which is connected to C terminal glows when inputs are A, B.

CONCLUSION:

- To add two bits we require one XOR gate(IC 7486) to generate Sum and one AND (IC 7408) to generate carry.
- To add three bits we require two half adders.

(b) Half-subtractor using logic gate

HALF SUBTRACTOR

AIM

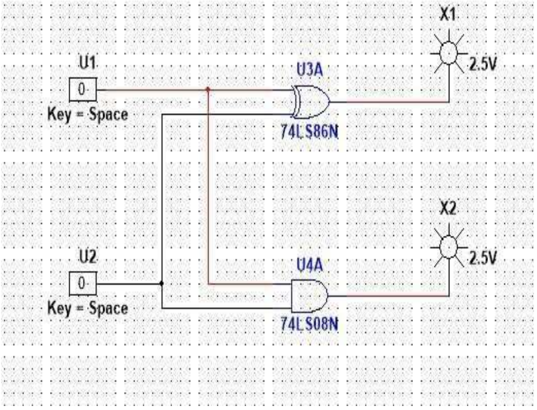
Design and verify the logic circuit of Half-subtractor using logic gate. OBJECTIVES:

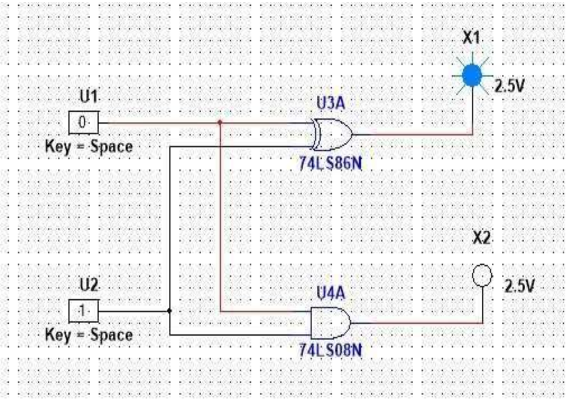
- To understand the principle of binary subtraction.
- To understand half-subtractor concept.
- Use truth table and Boolean Algebra theorems in simplifying a circuit design.
- To implement half-subtractor circuit using logic gates PROCEDURE:
- Collect the components necessary to accomplish this experiment.
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V.
- According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.

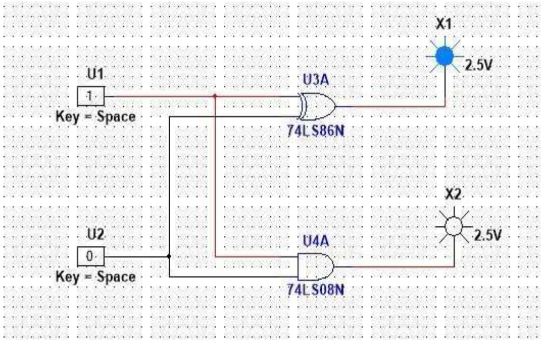
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of the bread-board
- Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs.

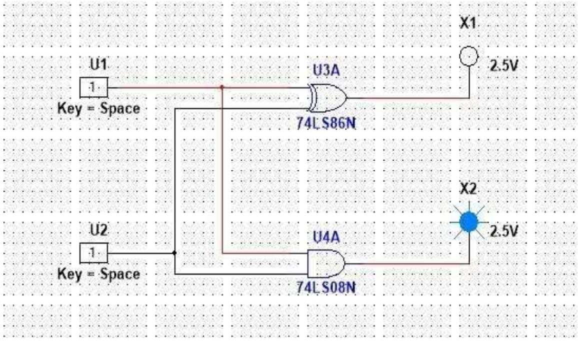
HALF SUBTRACTOR:

The half-subtractor is a combinational circuit which is used to per-form subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).









Observation table

A	B	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	o	0

RESULTS AND ANALYSIS:

Verified the truth table as follows. Verified the truth table of Full Subtractor as D = 1 i.e. LED which is connected to D terminal glows when inputs are, Y, BIN Verified the truth table of Full Subtractor as BOUT = 1 i.e. LED which is connected to BOUT terminal glows when inputs are X, Y, BIN

CONCLUSION:

- To add two bits, we require one XOR gate (IC 7486) to generate Difference and one AND (IC 7408) and NOT Gate (IC 7432) to generate Borrow.
- To add three bits, we require two half subtractor.

(c) J K Flip flop.

JK FLIP FLOP

AIM:

To Design and verify the truth table of J K Flip flop using IC 7473.

OBJECTIVES:

- To understand the principle of operation of sequential circuit
- To differentiate between combinational circuit and sequential circuit

. • To get familiar with basic Flip flops

- Determine the logic operation of JK flip flops.
- Connect and observe the state transition of JK as connected to the clock generator circuit.

PROCEDURE:

- Collect the components necessary to accomplish this experiment.

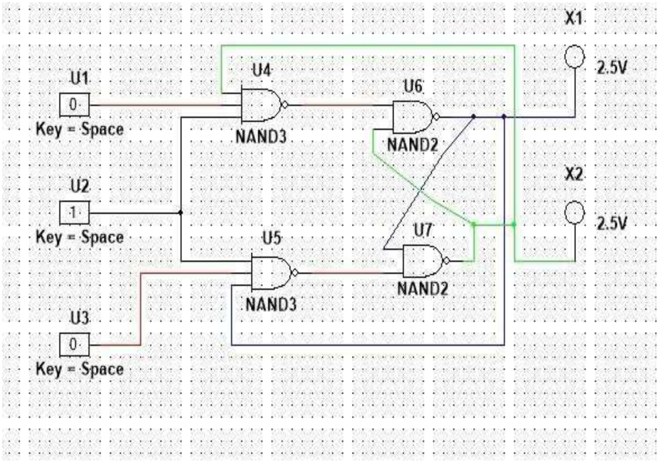
- Plug the IC chip into the breadboard.
- Connect the supply voltage and ground lines to the chips. PIN7 = Ground and PIN14 = +5V
- According to the pin diagram of each IC mentioned above, make the connections according to circuit diagram.
- Connect the inputs of the gate to the input switches of the LED.
- Connect the output of the gate to the output LEDs.
- Once all connections have been done, turn on the power switch of the breadboard
- Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF Apply the various combination of inputs according to the truth table and observe the condition of Output LEDs.

JK FLIP FLOP:

A flip-flop is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs

OBSERVATION TABLE:

CK	J	K	Q	Q_
1	0	0	-	-
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1



RESULTS AND ANALYSIS:

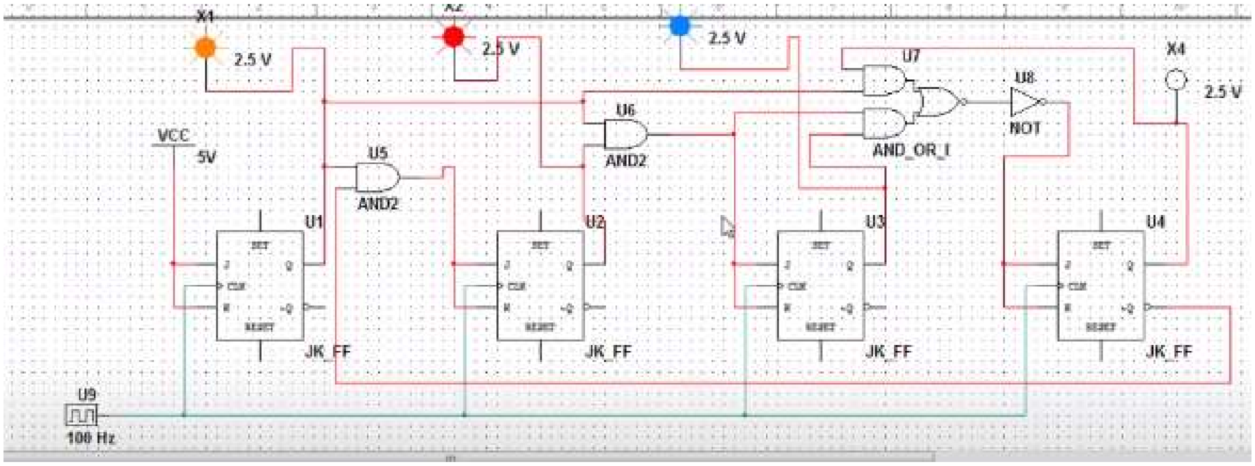
Flip-flops (FFs) are devices used in the digital field for a variety of purposes. Flipflops are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. In JK flip - flop, the letter J is for set and the letter K is for clear. When logic 1 inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa. Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs.) It can also be used for counting of pulses, and for synchronizing variably -timed input signals to some reference timing signal.

CONCLUSION:

The function table of JK flip flop using IC 7473 has been verified.

(e) Synchronous BCD Counter.

Synchronous BCD Counter



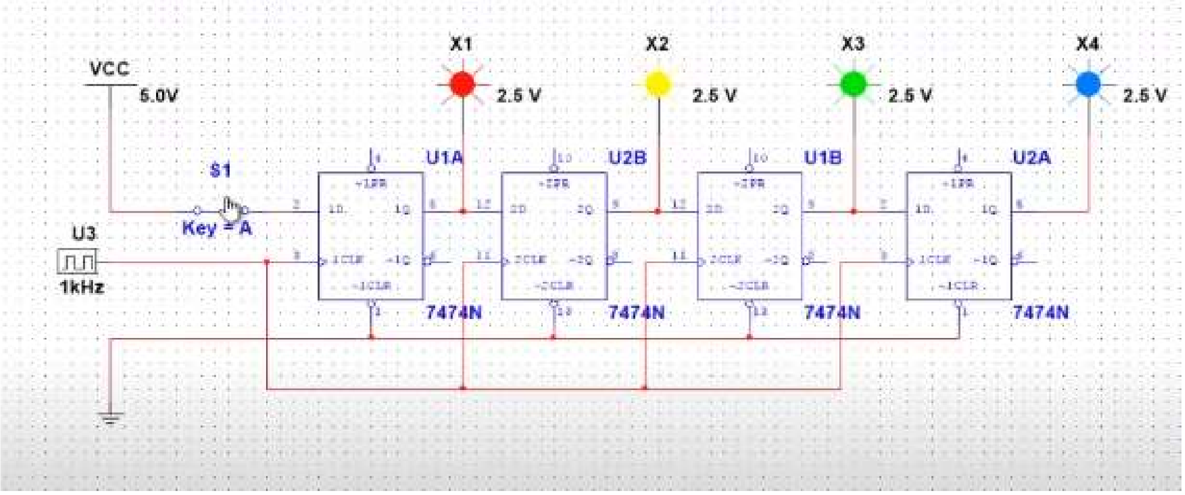
Present state				Next state				Output	FlipFlop inputs			
A	B	C	D	A	B	C	D	0	Ta	Tb	Tc	Td
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

(d) Serial in-serial Out shift register.

Serial-in to Serial-out (SISO) Shift Register

This **shift register** is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs Q_A to Q_D, this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.

The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.



Observation table.

CLK	INPUT	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	0
2	1	1	0	0
3	1	1	1	0