Question No ⇒ 01:

Signal spectrum, clocking noise immunity and cost can be used when evaluating digital to digital techniques. An excellent digital to digital encoding technique you pay for clocking to help determine the start and stop of each signal. As with any techniques you pay for what you get. The increased data rate directly correless with increased cost for technology.

Question NO ⇒ 02

For bipolar - AMI scheme a binary 0 is represented by no line signal, and a binary 1 is represented by a positive or negative pulse must alternat in polarity. For pseudoternary a binary 1 a is respresented by the absence of signal and a binary 0 by alternating positive and negative pulses.

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Question No ⇒ 03:-

In a scrambling technique sequence that would result in a constant voltage level on the line are replaced by filling sequences that will provides sufficient transitions for the receiver's clock to maintain. Synchronization The filling sequence must be recognized by the recieven replaced with the original data sequence.

Question No ⇒ 04:-

Along with bounty switch keying binary values tend to be display by mean of a couple of unique amplitudes associated with provider wavelength This Process will be vunerable to unexpected obtained adjustment and it is dysfunctional.

Question No ⇒ 05

To be precis the frequency components of a analog signal are repeated at the sample rate. The Sampling theoram states that a Cignalling can be exactly reproduced if it is sampled at the frequency F, where F is greater than twice the maximum frequency in the signal.

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Question No → 6:-

$$\frac{E_b}{N_0}_{dB} = 12\ dB - \frac{R}{B_T}_{dB}$$

For FSK and ASK from Figure 5.4

$$\frac{E_b}{N_0} = 14.2\ dB$$

$$\frac{R}{B_T}_b = 2.2\ dB$$

$$\frac{R}{B_T} = 0.6$$

For PSK From figure 5.4

$$\frac{E_b}{N_0 B_T} = 14.2\ dB$$

$$\frac{R}{B_T}_b = 0.8\ dB$$

$$\frac{R}{B_T} = 1.2$$

The result for QPSK must take into account that bound rate $D = R$?

Thus

$$\frac{R}{B_T} = 2.4$$

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Question No ⇒ 07:-

The CRC has more bit therefore provides more redundancy. It provides more information that can be used to detect error. Unlike the simple parity and longitudinal parity technique of error detection which produce high ratition of check bit error detection result.

Question No ⇒ 08.

For a long time signal bit error correction (with double bit error detection) has been the mainstay ECC technology for covering soft error in the cache. For the soft error rate that has been content with that signal bit correction can offer ECC will also be able to alert the signal and result in graceful shutdown or otherwise. However things are changing. As technology scaling continues, we are approaching the point where we will have a billion transistors on a signals peices of silicon with a big part some of these question and raises issues with the status quo.

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