Hilal

01 6966

Question = 01

Answer = 01

$$f = AB + (CD)E$$

N = . Series
+ Parallel

P = Parallel
+ Series

$f = \underline{A \cdot B + (C \cdot D)\ E}$

Hilal

02

6966

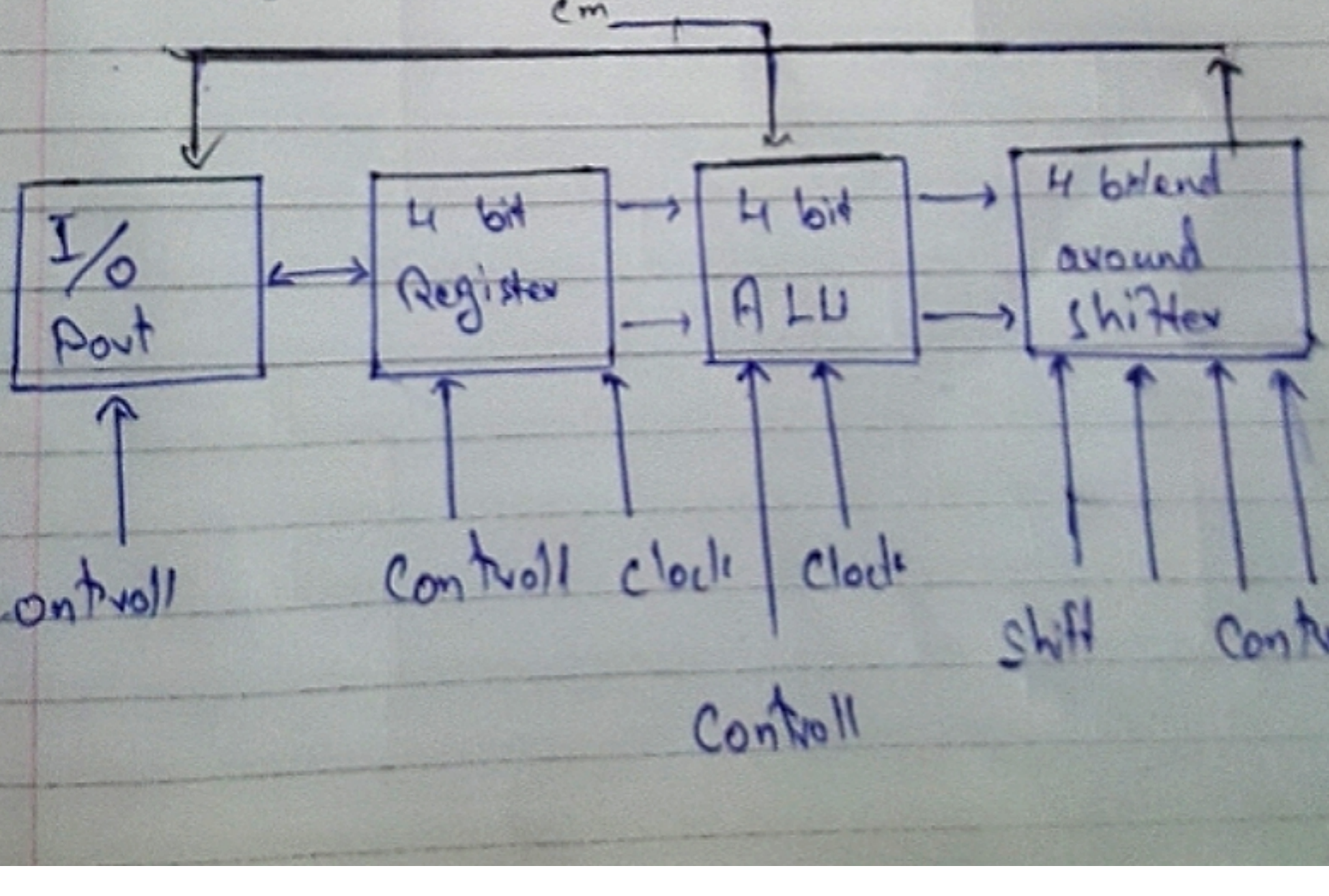
Question:.02.

Answer:

4 Bit Adder.

A 4 bit adder the fast Carry Generator Description. These full adders Perform the addition of two 4 bit bin numbers. The sum (Σ) out put Provided for each bit & the resultant Carry (c4) is obtaind from the fourth bit. These adders feature full internal look Ahead across all four bits.

① Design Subsystem Consideration.



Hilal G966 03

* Design of 4 bit adder.

Input			Out · Put	
Ak	Bk	Ck-1	Sk	Ck
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Hall. 6966 04

Question. 203. Part (A)

Answer = 03 : Issues VLSI Design.

In all design process : a logical and systematic approach is essential. This is a particular do in the case of the design of a VLSi System which could take so long as to render the all system obsolete before it is often the drawing board.

(*) But now some p design requirement is there.

(1) Define the requirement. (Properly & Carefully)

(2) the overall architecture Subsystem Partition.

(3) Communication Path Carefully in order to develop Sensible interrelationship b/w system.

4) A floor plan of how the system is to map onto Silicon. All alternative blw 2, 3, & 4 necessary.

5) Regular structure of design largely matter of repetition.

6) Suitable stick or symbolic diagrams of the leaf cells of the subsystem.

7) Convert each cell to layout..

Hilal 6966 05 06

Question = 03) Part (B)

Answer:

Simple Parity-check code

The simple parity check code is the most famillion error-detecting code. in this code, a (n, bit data word is changed to an n-bit code word where n = k+1

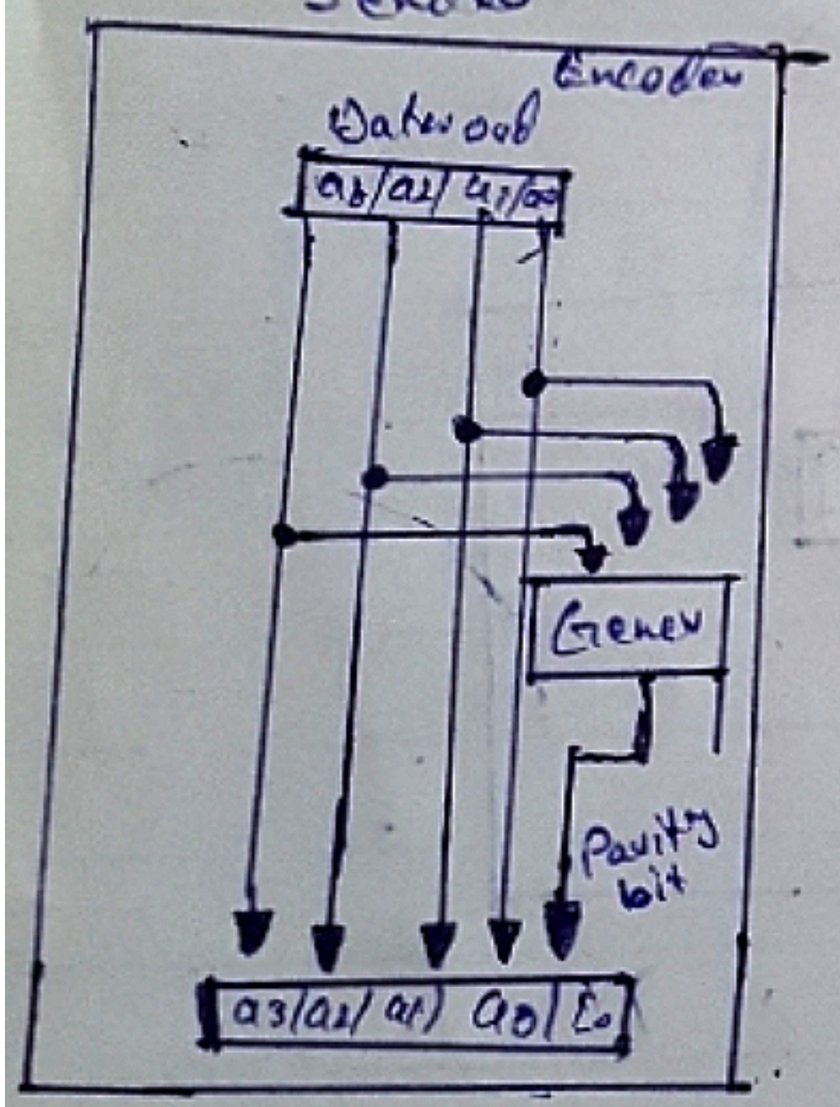
The extra bit, is selected to make the total number of 1s.

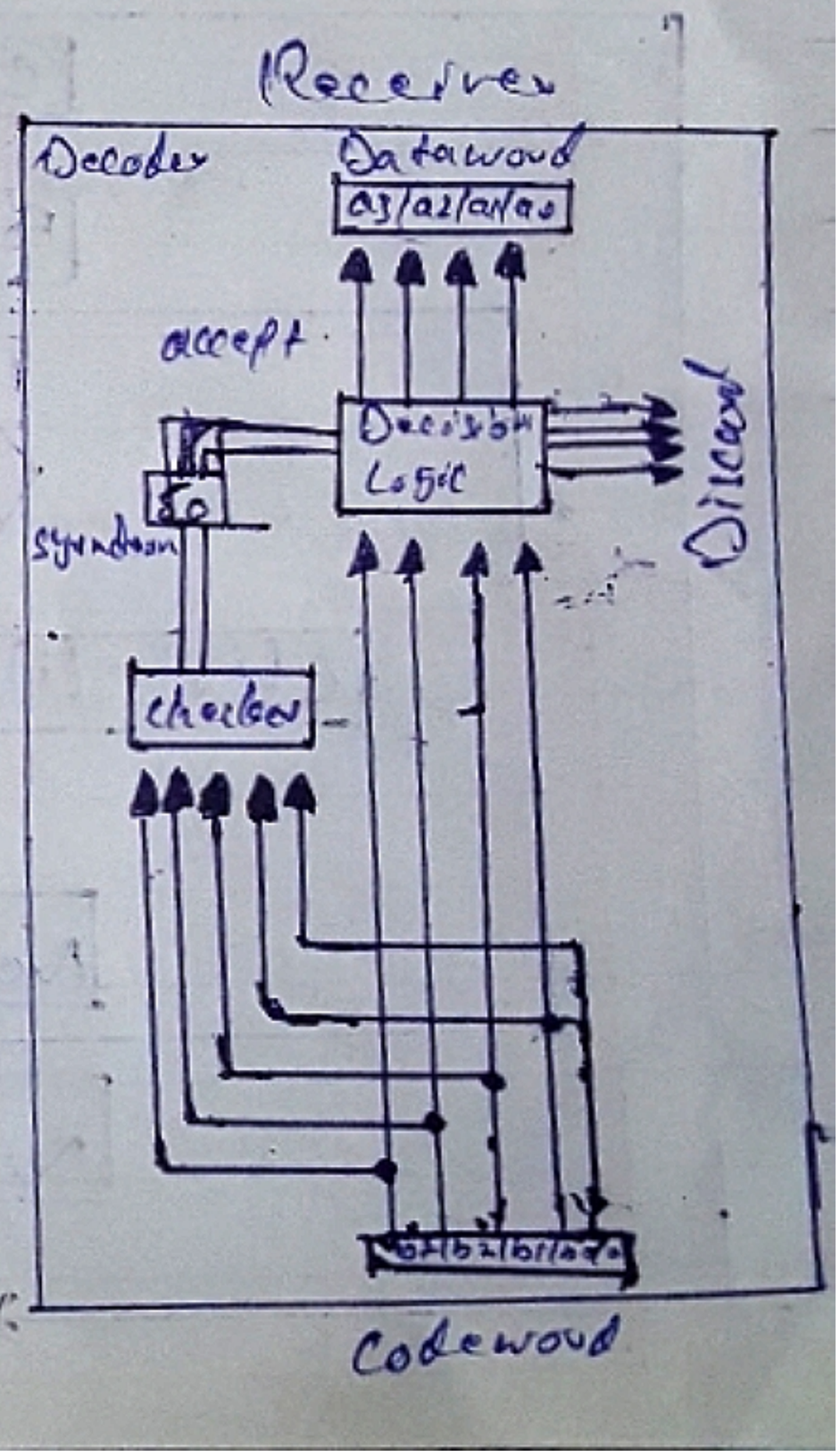
The minimum Hamming Distance for this category is dmin = 2. which mean the code is single bit error detecting code.

* it can not correct any error.

Diagram:

* The Following Possible Structure of an encoder (at the Sender and decoder) at the receiver:





Ex: #

The sender sends data word 1011. The code created from this data word 1011, which is sent to receiver we examine five cases:

(1) No error occurs, received code word is 1011.
Zero data word 1011 created.

(2) One single bit error change a1.
received code 1111. Syndrome is 1.
No word is created,

(3) One single bit error changes v0.
received 1110 the syndrome is 1.

(4) Error changes v0. and second a3.
Received code 0011 syndrome.
data word 0011 is created
the receiver.

Hilal 6966 09

(5) Three bits a3, a2, and a1 change errors. a received code 0101. the syndrome is?

(*) 7 bit bytes are put seperate, rows and columns and calculated.

1	1	0	0	1	1	1	1
1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	1

Parity

Row

Column parity

Question : 04.

Answer 04.

The inverter have alway lower Limit of the Power depends on the Sum of the threshold voltages of the nMOS and VDD.

- Logic function is implemented by pull down network only.
- Full swing out-puts (V OL = GND and V OH = VDD).
- Non - ratioed.
- faster Switching speeds.
- Inverter (Resistance Load) mu-nC-ox = 25 mu A/V^2

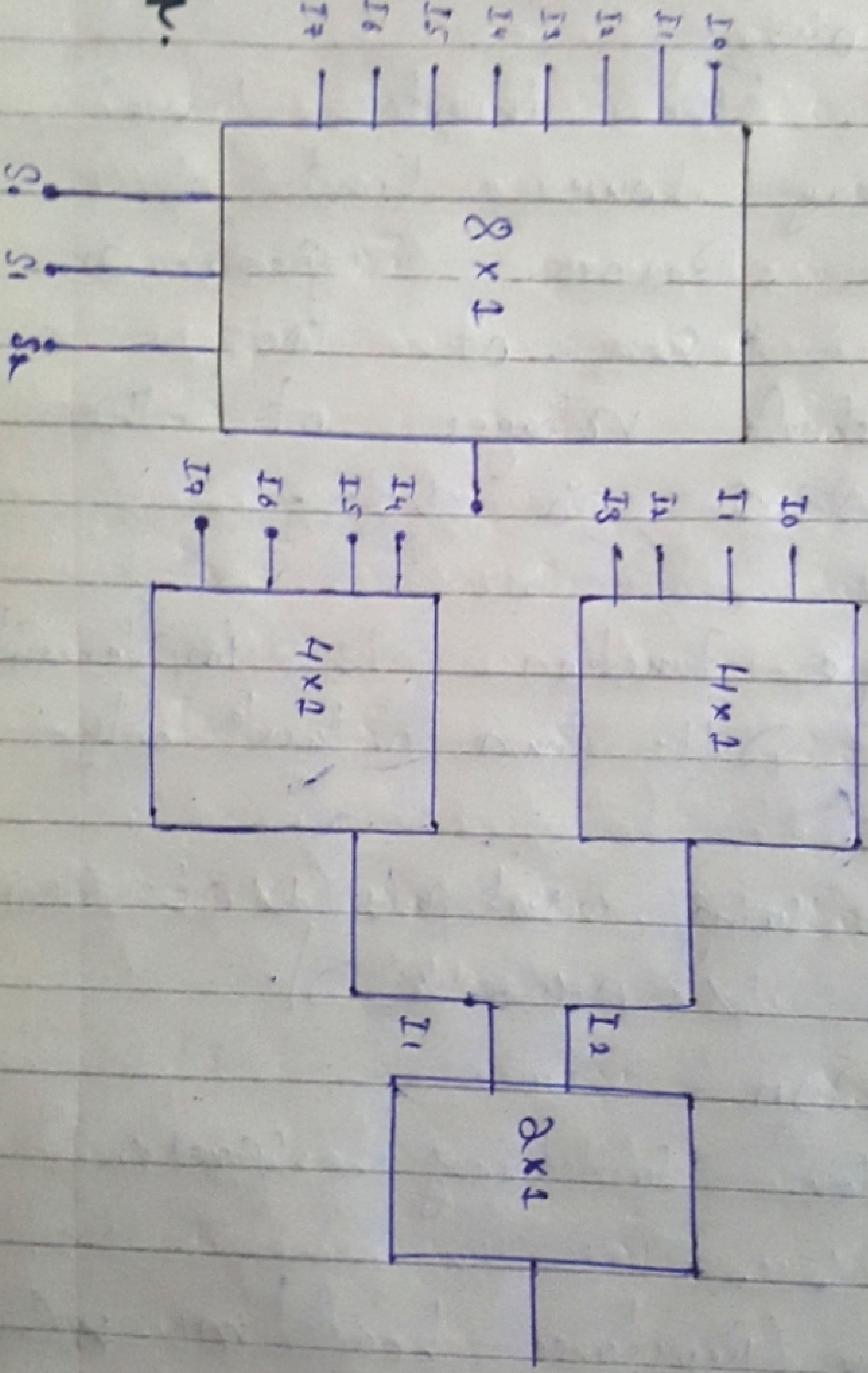
W/L = 10 V = T = Iv V-L = Low (0)

right awow V_0 = 5 v (xM)

T = C_L ΔV / I .

~~[-0 = 1 (11 / 9.8.~~

Question = 05



8x1 Mux

Truth Table.

Sa	S1	S0	output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4 x 1

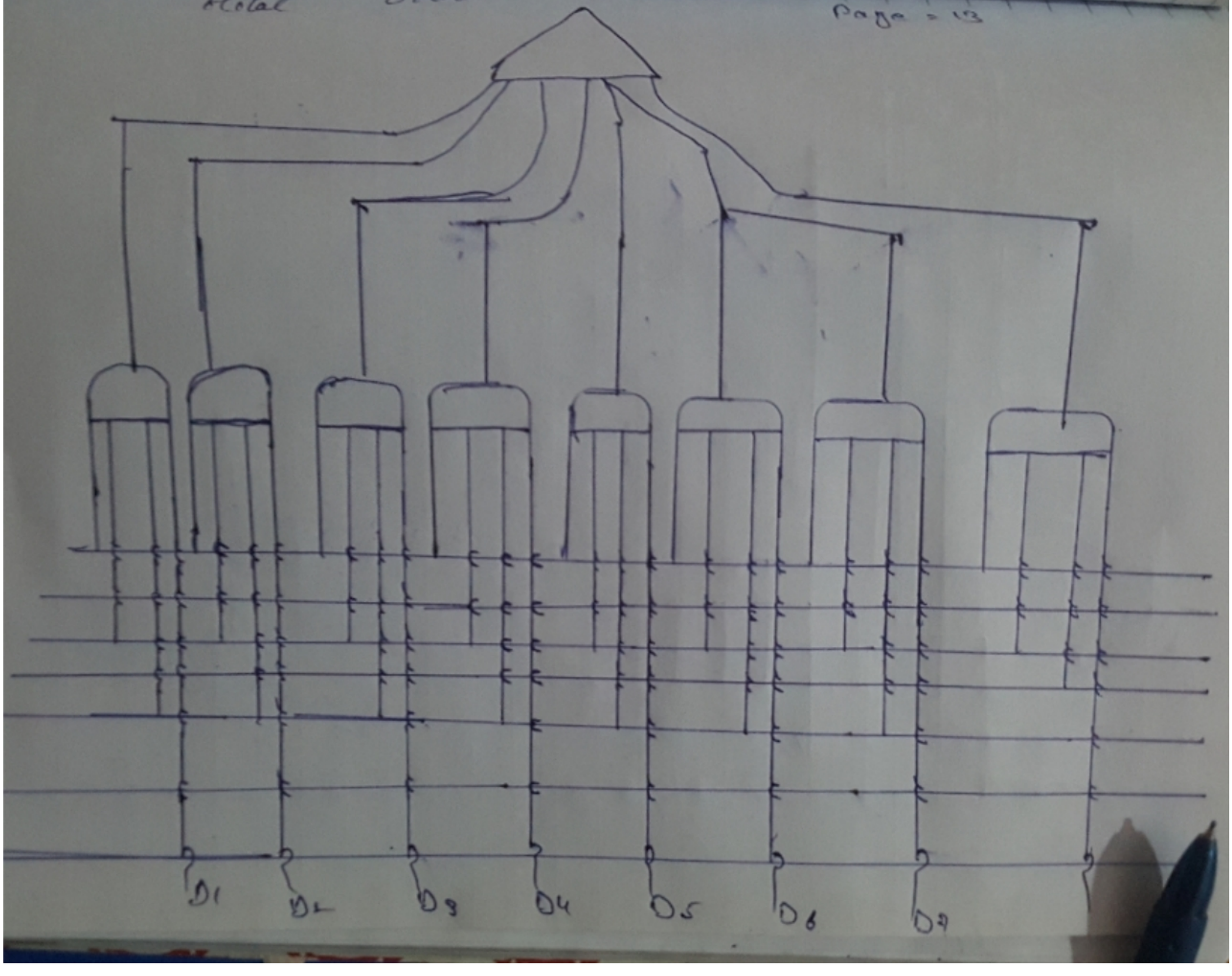
S1	S0	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2 x 1

S1	S0	y
0	0	I_0
0	1	I_1

Hotel 6866

Page = 13



Hilal 6966 14

★ 8 x 1 Mux by Voz Method

$I_0 = S_1 \quad S_1 \quad S_0$

$I_1 = S_1 \quad S_1 \quad S_0$

$I_2 = S_1 \quad S_1 \quad S_0$

$I_3 = S_1 \quad S_1 \quad S_0$

$I_4 = S_2 \quad S_1 \quad \hat{S}_0$

$I_5 = S_2 \quad S_1 \quad \hat{S}_0$

$I_6 = S_2 \quad \hat{S}_1 \quad \hat{S}_0$

$I_7 = S_2 \quad \hat{S}_1 \quad \hat{S}_0$