IQRA NATIONAL UNIVERSITY

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*Assignment No : 2nd*

*Subject : Computer Architecture*

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Q1 Give answer to each of the following.

(A) Discuss different desktop application that require the great power of contemporary microprocessor based systems?

Ans Different Desktop application that require the great power of contemporary microprocessor based system are.

Image processing
Three-dimensional rendering
speech recognition
video conferencing
Multimedia authoring
voice and video annotation of files
simulation modelling

(B) Discuss the techniques used in contemporary processor to increase speed:

Ans ⇒ The techniques used in contemporary processor to increase speed are following:

Pipelining ⇒ Pipelining enables a processor to work simultaneously on multiple instruction by performing a different phase for each of multiple instruction at the same time.

Branch Prediction ⇒ Branch prediction potentially increases the amount of work available for the processor to execute.

Super scalar execution ⇒ This is ability to issue more than one instruction in every processor clock cycle. in effect multiple parallel pipelines are used.

Speculative execution ⇒ This enables the processor to keep the execution engines as busy as possible by executing instruction that are likely to be needed.

Data flow Analysis ⇒ The processor analyses which instruction are dependent on each other results or data to create an optimized schedule of instruction.

(c) Discuss the problems created due to increase in clock speed and logic density of the processor?

Ans: Discuss the problems created due to increase in clock speed and logic density of the processor are

Power :- As the density of logic and the clock speed on chip increase so the power density increase and also dissipated the heat.

RC delay :- The speed which electrons can flow on a chip b/w transistor is limited by the resistance and capacitance of the metal wires connecting them; specifically delay increase as the RC product increase.

Memory latency :- Memory access speed (latency) and transfer speed (throughput) lag processor speeds.

(d) Discuss the speedup of a program using multiple processor compared to a single processor using Amdahl's Law.

Ans: The speedup using a parallel processor with N processor that fully exploits the parallel portion of the program is as follows:

Speed up = Time to execute program on a single processor / Time to execute program on N parallel processor.

$$= T(1-f) + T.f / T(1-f) + Tf/N$$

$$= 1/(1-f) + f/N$$

(5): Discuss the multicore, MIC and GPGPU in detail:

Ans: Multicore: The use of multiple processor on the same chip provides the potential to increase performance without increasing the clock rate.
With two processor larger caches are justified.

- MIC: Leap in performance as well as challenges in developing software to exploit such a larger number of cores. The multicore and MIC strategy involves a homogeneous collection of general purpose processor on a single chip.

GPGPU: The core designed to perform parallel operation on graphics data. Traditionally found on plug-in graphics card. It is used to encode and render 2D-3D graphics as well as process video.

Q2 Solve each of the following.

(A) A benchmark program is run on a 60 MHz processor. The execute program consist of 104000 instruction execution with the instruction mix and clock cycle count given below. Determine the effective CPI MIPS rate and execution time for this program.

| Instruction Type | Instruction count | cycles per instruction |
|---|---|---|
| Integer arithmetic | 46000 | 1 |
| Data transfer | 33000 | 2 |
| Floating point | 16000 | 2 |
| control transfer | 9000 | 2 |

Ans es Effective CPI es

$$CPI = (1 * 46000) + (2 * 33000) + (2 * 16000) + (2 * 9000) / 100$$

$$CPI = 162000 / 100$$

$$CPI = 1620$$

MIPS Rate es 60 MHz / 1620 * 10^6

$$MIPS\ rate = 60 / 1620$$

$$MIPS\ Rate = 0.037$$

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Execution Time =

$T = IC / MIPS * 10^6$

$T = 104000 / 37 * 10^6$

$T = 2811 * 10^{-3}$

$T = 2811$ sec

(B) Consider two different machines with two different instruction sets both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

| Instruction Type | Machine A: Instruction Count | Machine A: Cycles per Instruction |
|---|---|---|
| Arithmetic and Logic | 8 | 1 |
| Load and Store | 4 | 3 |
| Branch | 2 | 4 |
| others | 4 | 3 |

| | | |
|---|---|---|
| Arithmetic and logic | 10 | 1 |
| Load and Store | 8 | 2 |
| Branch | 2 | 4 |
| others | 4 | 3 |

Determine effective CPI, MIPS and execution time for each machine.

Ans (a) For Machine A

CPI = (1*8+3*4+4*2+3*4)*10^6 / (8+4+2+4)*10^6

40*10^6 / 18*10^6

CPI = 2.22

MIPS rate =

MIPS Rate = 200 MHz / 2.22*10^6

MIPS Rate = 200*10^6 / 2.22*10^6

MIPS Rate = 90

T = Ic / (MIPS * 10^6)

T = 18*10^6 / 90*10^6

T = 0.2 sec

For Machine B CPI =

= (1*10+2*8+4*2+3*4)*10^6 / (10+8+4+4) *10^6

CPI = 46/24

CPI = 1.92

MIPS rate = 200 MHz / 1.92 * 10^6

MIPS rate = 200 * 10^6 / 1.92 * 10^6

**MIPS Rate = 104**

T = Ic / MIPS * 10^6

T = 24 * 10^6 / 104 * 10^6

**T = 0.23 sec**

Ans 5 D)

Since we have the same instruction mix that means the additional instruction for each task could be allocated appropriately between the instruction type Therefore the following table be gotten

| Instruction Type | CPI | Instruction Mix |
|---|---|---|
| Architecture and logic | 1 | 60 % |
| Load/Store with cache hit | 2 | 18 % |
| Branch | 4 | 12 % |
| Memory reference with cache miss | 12 | 10 % |

The average CPI = (1×0.6) + (2×0.18) + (4×0.12) + (12×0.1)

CPI = 2.64

Therefore CPI has been increased since the time for memory access is also increased.

b) MIPS = 400/2.64 = 152

There is a corresponding drop in the MIPS rate

c) The speedup factor equal to the ratio of the execution times.

The execution time is calculated as the following

$T = I_c / (MIPS \times 10^6)$

For one process $T_1 = (2 \times 10^6) / (2 \times 10^6)$

$T_1 = 1$ ms

For 8 processor each process executed 1/8 of the 2million instruction plus the 25,000

$T_8 = 2 \times 10^6/8 + 0.025 / 2 \times 10^6$

$T_8 = 1.8$ ms