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Department BS.CS 4th Semester

Assignment NO 2nd

Subject : Computer Architecture.

Q.1 Give answer to each of the following.

(A) Discuss different dekstop application that require the great power of contemporary microprocess-based system?

Ans: Different desktop application that require the great power of based system are
Image procesing
Three dimesional rendering
Speech recognition
Video conferencing

Multimedia authoring.
Voice and vedio annotation of files.
Simulation modelling.

(B) Discuss the techiques used in contemporary processors to increase speed?

Ans: The techniques used in contamporary processors to increase speed are following.

Pipelining:

Pipelining enables a Processor to work Simultaneouly on multiple intructions by performing a different phase for each of the multiple instruction at the same time.

Branch predication:

Branch Predication potencially increses

the amount of work available for the processor to execute.

SuperScalar execution:

This is the ability to issue more then one instruction in very processor clock style. In effect multiple parallel pipelines are used.

Data flow analysis:

The processor analyzes which instruction are dependent on each other's results, or data to create an optimized Schedule of instructions.

Speculative execution:

This enable the processor to keep its execution engines as busy a possible by executing instruction that are likely to be needed.

(c) Discuss the problems created due to increase in clock speed and logic density of the processor?

Ans. Discuss the problem created due to increase in clock speed and logic density of the processor are

Power:

As the density of logic and the clock speed on a chip increase, so the power density increase and also dissipated the heat.

RC delay:

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wire connecting them; specially delay increases as the RC product increase.

Memory latency:
Memory access speed (latency) and transfer speed (throughput) lag processor speeds.

(D) Discuss the speedup of a program using multiple processors compared to a single processor using Amdahl's Law?
The speedup using a parallel processor with N processors that fully exploits the parallel portion of the program is as follow.
Speedup = Time to execute program on a single processor / Time to execute on N parallel processors.
$= T(1-7) + T7/T(1-7) + T7/N$
$= 1/(1-7) + f/N$

(E) Discuss the multicore, MIC, and GPGPU in detail?

Ans: Multicore:

- The use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.
- Strategy is to use two simpler processors on the chip rather than one more complex processor.
- With two processors larger caches are justified.
- As caches became larger it made performance sense to create two and then three levels of cache on a chip.

MIC:

- Leap in performance as well as the challenge of software to exploit such a large number of cores.
- The multicore and MIC strategy involves a homogeneous collection of general purpose processor on a signal

GPUS:

- Core designed to perform Parelled operation on graphic data.
- Traditionally found on a plug-in graphics card, it is used to encode and render 2D and 3D graphics well as process video.
- Used as vector processors for a variety of applications that require repetive computations

Q2: Solve each of the following:

Ⓐ A benchamark program is run on a 60 MHz processor. The execute program consist of 10,000 instruction executions with the instruction mix and clock cycle count given below. Determine the effective CPI, MIPS rate, and

and execution time for this program.

Instruction type	Instruction count	cycle per Instruction
Integer airthmetic	46,000	1
Data transfer	33,000	2
Floating Point	16,000	2
control transfer.	9,000	2

Ans: Effective CPI:

$CPI = (1 * 46000) + (2 * 33000) + (2 * 16000) + (2 * 9000)$.

$CPI = 162000/100$

$CPI = 1620$

MIPS Rate:

$MIPS\ rate = 60MHz/1620 * 10_6$

$MIPS\ rate = 60 * 10_6 / 1620\ 10_6$

$MIPS\ rate = 60/1620$

$MIPS\ rate = 0.037$

Execution Time:

$T = Ic / (MIPS * 10_6)$

$T = 104000 / 0.037 * 10_6)$

$T = 104000/37 * 10_3$

$T = 2811 * 10_3 \Rightarrow T = 2.811 Sec.$

(B) Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurment are recorder on the two machines running a given set of benchamark Programs:

Instruction type	Instruction count million	cycle Per Instruct
Arithmetic logic	8	1
Load and Store	4	3
Brach	2	4
Other	4	3
Arithmetic logic	10	1
Load and Store	8	2
Brach	2	4
others	4	3

For Machine A:

CPI = (1*8 + 3*4 + 4*2 + 3*4) * 10^6 / (8+4+2+4) * 10

(10)

CPI = $40 * 10_6 / 18 * 10_6$
CPI = 2.22.

MIPS rate = $200MHz / 2.22 * 10_6$
MIPS rate = $200 * 10_6 / 2.22 * 10_6$
MIPS rate = 90

$T_1 = IC / (MIPS * 10_6)$
$T = 18 * 10_6 / 90 * 10_6$
T = 0.2 Sec

For Machine B:

$CPI = (10 * 1 + 2 * 8 + 4 * 2 + 3 * 4) * 10^6 / (10 + 8 + 2 + 4) * 10_6$
CPI = 46/24.
CPI = 1.92

MIPS rate = $200MHz / 1.92 * 10_6$
MIPS rate = $200 * 10_6 / 1.92 * 10_6$
MIPS rate = 104

$T = IC / (MIPS * 10_6)$
$T = 24 * 10_6 / 104 * 10_6$
T = 0.23 Sec.

(c) Early examples of CISC and RISC design are the VAX 11/780 and the IBM RS/6000, respectively. Using a typical benchmark program the following machine characteristics result.

Ans:

Processor	Clock Frequency (MHz)	Performance (MIPS)	CPU Time (Second)
VAX 11/780	5	1	12x
IBM RS 6000	25	18	x

The final column shows that the VAX required 12 times longer than the IBM measured in CPU time.

(a) What is the relative size of the instruct count of the machine code for this benchmark Program running on the two machine?

Ans: The MIPS rate could be computed as the following:

MIPS rate = IC / T * 10_6

IC = MIPS rate * T * 10_6

Now by computing the ratio of the instruction count of the IBM RS/6000 to the VAX 11/780 which is:

$18*1x*10_6 / 1*12x*10_6$

$\Rightarrow 18/12$

$= 1.5$

(b) What are the CPI values for the two machines?

Ans: Regarding to the VAX 11/780 the

$CPI = (5MHZ)/(1*10_6) = 5*10_6/1*10_6$

$:= 5/1 = 5.$

Regarding to the IBM Rs 6000 the

$CPI = (25MHZ)/(18*10_6) = 25*10_6/18*10_6$

$= 25/18 = 1.4.$

(D) Ans: (a): Since we have the same instruction mix, that means the additional instructions for each task could be allocated appropriately between the instruction types. Therefore, the following table be gotten:

Instruction Type	CPI	Instruction Mix
Arithmetic and logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

The average CPI = $(1 \times 0.6) + (4 \times 0.12) + (4 \times 0.12) + (12 \times 0.1) = 2.64$.

Therefore, the CPI has been

increased Since the timer for memory access is also increased.

(b): MIPS = 400/2.64 = 152
There for a corresponding drop in the MIPS rate.

(c): The speedup factor equals to the radio of the execution times. The execution time is calculated as the following $T = Ic / (MIPS * 10_6)$
For the Processor $T_1 = \frac{(2 * 10_6)}{(178 * 10_6)}$
$\Rightarrow$ 11 ms.

For the 8 Processors, each Processor executes 1/8 of the 2 million instruction Plus the 25,000
$T_8 = 2 * 10_6 \div 8 + 0.025 * 10_6 / 152 * 10_6$
$T_8 = 1.8$ ms.
Therefore we have:
Speedup = Time te exute Program on a single Processor / Time to excute Program on N Pallel Processors.

Speedup = 11/1.8.
Speedup = 6.11.

(d): By depending on the information given, it is not obvious how to quantify thes effect in Amdahl's equation. Therefore, if it is Supposed that the fraction of code, which is Parallelizable is ? = 1 then Amdahl's law decreases to speedup = N=8. Therefore, The actual speedup is only about 75% of the theoretical speed up.