Department of Electrical Engineering
Assignment 2
Date: 09/05/2020

Course Details

Course Title: vlsi **Module:**
Instructor: Engr.zulqarnain **Total Marks:**

Student Details

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Q1.		Consider a resistive load inverter circuit with V_{DD} = 5v, K'n= 20 uA/V^2 , V_{To} =0.8V, R_L = 200 k(Ohm), W/L = 2 Calculate the critical voltage s V_{OL}, V_{OH}, V_{IL}, V_{IH} on the VTC and find the noise margins of the circuits?
Q2.		Design a CMOS logic layout given the following function F= $\overrightarrow{\overline{(AB+C)B+D}}$
Q3.		What is MOS Inverter? Also draw the circuit diagram of MOS Inverter
Q4		Write a note on Depletion load NMOS Inverter.

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Q1 Consider a resistive load inverter circuit with

$V_{DD} = 5V$ $k_n = 20\ \mu A/V^2$ $V_{TO} = 0.8V$
$R_L = 200\ k\Omega = 200\ W/L$
Calculate the critical voltage V_{OL}, V_{OH}, V_{IL} V_{IH} on the VTC and Find the noise margins of the CKT?

Sol:- (i) $V_{OH} = V_{DD}$

$$\boxed{V_{OH} = 5V}$$

$$\Rightarrow \text{(ii)}\quad V_{OL} = V_{DD} - V_T + \frac{1}{K_n R_L} - \sqrt{\left(V_{DD} - \frac{V_T + L}{K_n R_L}\right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$\Rightarrow \text{But } k_n = k_n' \frac{W}{L}$$

$$= 20 \times 10^{-6} \times 2$$

$$k_n = 40 \times 10^{-6}$$

$$V_{OL} = 5 = 0.8 + \frac{1}{40 \times 10^{-6} \times 200 \times 10^3} - \sqrt{5 - 0.8 + \frac{1}{40 \times 10^{-6} \times 200 \times 10^3}} - \frac{2 \times 5}{40 \times 10^{-6} \times 200 \times 10^3}$$

$$V_{OL} = 4.325 - 2.174$$

$$\boxed{V_{OL} = 2.151V}$$

(iii) $V_{IL} = V_T + \frac{1}{40 \times 10^{-6} \times 200 \times 10^{3}}$

$V_{IL} = 0.925^{-}$

(iv) (a) $V_{IH} = V_T + \sqrt{\frac{8}{3} \frac{V_{DD}}{K_n R_L}} - \frac{1}{K_n R_L}$

$= 0.8 + \sqrt{\frac{8}{3} \times \frac{5^{-}}{40 \times 10^{-6} \times 200 \times 10^{3}}} \quad \frac{-1}{40 \times 10^{-6} \times 200 \times 10^{3}}$

$= 0.8 + 1.289 - 0.125$

$= \boxed{V_{IH} = 1.96V}$

Now noise margin

$\Rightarrow N_L = V_{IL}$ val

$= 0.925 - 2.15^{-}$

$\boxed{N_L = -1.225^{-}}$

$\Rightarrow N_H = V_{OH} - V_{IH}$

$= 5^{-} - 1.289$

$\boxed{N_H = 3.711}$

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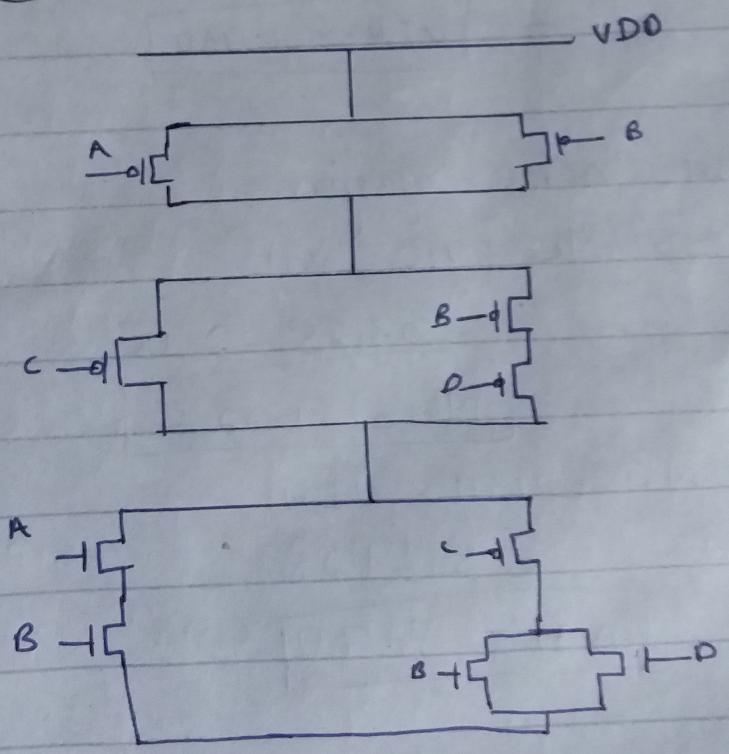
Q2 Design a CMOS Logic Layout given the following fonction

$$F = \overline{(AB + C)B + D}$$

Solution :→



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Q4 Write a note on Depletion Load NMOS inverter

Ans => In Integrated circuit depletion Load NMOS is a form of digital Logic family that use for a single Power supply voltage earlier NMOS Logic families that needed more then one different power Supply voltage

=> A Though manfacturing these integrated circuits reaurred addition processing steps elimination of extra power supply and then Improved switching Speed made this Logic faimlly the prefford Choise for many microprossesr and other logic elements. Some depletion Load NMOS design are still produced typically in Parallel with newer CMOS counter Part.