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Paper Computer Architecture

Dept BS(cs)

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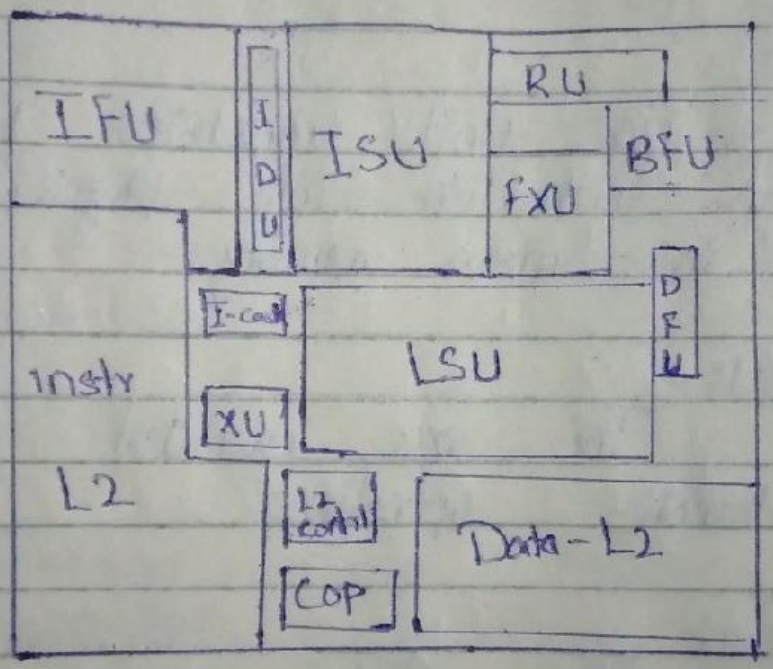
Q1

Ans:



Function of each subareas:-

ISU :-

Determine the sequence in which instruction are executed in what is referred to as a Superscalar architecture.

IFU:-

Logic for fetching instructions.

IDU:-

The IDU is fed from the Ifu buffers and is responsible for the parsing and decoding of all Architure operation codes.

LSU:-

It is responsible for handling all types of operand accesses of all lengths, modes, and formates as defined in the z/Architure.

XU:-

This unit translates logical addresses from instruction into physical addresses in main memory.

FXU:-

The fxu executed fixed point arithmetic operations.

BFU:-

The BFU handles all Binary and hexadecimal floating-point operations as well as fixed Point multiplication operations.

DFU:-

The DFU handles both fixed Point and floating-Point operation on numbers that are stored as decimal digit

RU:-

The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signal etc.

CoP3:-

The CoP is responsible for all data compression and encryption function for each core.

I Cache:-

This is 64-KB L_1 instruction cache, allowing IFU to prefetch instruction before they are needed.

L_2 Controls:-

This is control logic that manages the traffic other than instruction.

Instr L_2:-

A 1-MB L_2 instruction cache.

Ans

IAS Operations:-

IAS operation by repetitively Performing an instruction Cycle.
Cycle Consist of Two Subcycles.

1) Fetch Cycle:-

During fetch cycle the oper opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. this instruction may be taken from the IBR. It can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR and MAR.

2) Execute Cycle:

Control Circuitry interpret the ~~opcode~~ opcode and executed the instruction by Sending out the appropriate Control Signal to Cause data to be moved or an operation to be performed by the ALU.

Ans:- (C)

The term embedded System refers to the use of electronic and Software within a product. supposed to a general purpose Computer, such as laptop. Today many device are use to electronic power have an embedded computer system. Different embedded system are use to daily life. cell phone, microwave, machine etc.

Ans:- D)

Different desktop application that require the great power of Contemporary microprocessor based System are.
Image Processing
Speech recognition.
Multimedia Authoring
Voice and video annotation of files
Simulation modeling.

Ans:- E)

The Technique used in Contempory processor to increase speed are following.

Pipelining:- A pipelining is a series of stage, where some

Work is done at each stage in Parallel. The stage are connect one to the next to form a pipe - instruction entre at one end progress through the stages, and exist at the other end.

Branch Predictions:-

Branch Prediction techique because it does not rely on information about the dynamic history of code executing.

Superscale Executions:-

It is the ability to issue more than one instruction in every processor clock cycle. In effect multiple Parallel Pipelines are used

Data flow analysis:-

The Processor analyses which instruction are dependent on each other result or data, to create an optimized Schedule of instruction.

Speculative executions:-

This enables the Processor to keep its execution engines as busy as possible by executing

instruction that are likely to be needed.

Ans:- f)

The Problem created due to increase in clock speed and logic density of the processor are.

Power:-

As the density of logic and the clock speed on a chip increase. So does the Power density it difficulty of dissipating the heat generated on high-density high speed chips is becoming serious design issuse.

RC delays:-

The speed at which electrons can flow on a chip between transistor is limited by the resistance and capasitance of them specifically delay increase as the RC Product increase.

Memory latency and throughputs:-

Memory access speed transfer speed (throughput) lag Processor speed.

Ans :- G)

Consider a program running on a single processor such that a fraction (1-f) of the execution time involves code that is inherently sequential. and a fraction of that involves codes that is infinitely parallelizable with no scheduling overhead.

$$\text{Speedup} = \frac{\text{Time to execute program on a signal Processor}}{\text{Time to be execute Program on N Parallel processor}}$$

$$\text{Speedup} = \frac{T(1-f) + Tf}{T(1-f) + \frac{Tf}{N}} = \frac{1}{(1-f) + \frac{f}{N}}$$

Ans: H)

Multicore:

The use of multiple Processor on the same chip. also reffered to as multiple cores or multicore provides the potential to increase performance without increasing the clock rate. If the software can support the effective use of multiple

then doubling the number of Processor almost double performance.

Two Core chip were quickly followed by four-core chips, then 8, then 16, and so on.

MIC:-

The leap in performance as well as the challenges in developing Software to exploit such a large number of Core has led the introduction of new term called many integrated Core (MIC) The multicore and MIC strategy involves a homogenous Collection of general purpose Processor on a single chip.

GPU:-

A GPU is a Core designed to perform parallel operation on plug in graphics cards and graphic data.

It is used to encode and render 2D and 3D graphics as well as process video.

GPU perform ~~parallel~~ parallel operation on multiple sets of data, they are increasingly being used as vector processor for a variety application that require repetitive computation.

Ans: D

Quick Path Interconnect protocol layers.

In this layer, the packet is defined as the unit of transfer.

The packet content definition is standardized with some flexibility allowed to meet differing market segment requirements.

One key function perform in this layer is a ~~cache~~ Cache Coherency protocol, which deals with + making sure that main memory held in multiple caches consistent.

Ans:(ii)

Physical and Logical Architecture of PCIs:-

Root Complex:-

it is also called Chipset or a host bridge which Connects the processor and memory Subsystem to the PCI Express Switch fabric. Comprising one or more PCI. and PCI Switch devices.

The root Complex acts as a buffering device to deal with differences in data refer between I/O Controllers and memory and Processor components

PCIe links from the chipset may attach to the following kinds of devices that implements PCIe.

Switch:-

The Switch manages multiple PCIe Streams.

PCIe Endpoints-

An I/O device or Controller that implements PCIs. Such as a Gigabit ethernet Switch a graphics disk interface etc.

Legacy endpoints

Legacy endpoint Category is intended for existing designs that have been migrated to PCI Express and it allows legacy behaviour such as use of I/O space and locked transactions.

PCI-X / PCI bridges

Allows older PCI devices to be connected to the PCI-based System.

(Q) 2

Ans: Structure Components of Computer:

There are four main structural components of computer.

Central Processing Unit (CPU):-

It controls the operation of the computer and performs its data processing function often simply referred to as Processor.

Main Memory:-

It is stores data.

I/O:-

It moves data between the computer and its external environment.

System Interconnection:

Some mechanism that provides for communication among CPU, main memory and I/O is called system interconnection. Its example of system interconnection is by means of a system bus.

Ans: B)

The characteristics of computer family are as follows:

Similar or identical instruction set:

In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family this means that program can move up but not down.

Similar or identical operating system:

The same basic operating system is avialable for all family members.

Increasing speed:

The rate of instruction execution increases in going from lower to higher family member.

Increasing number of I/o Ports:

The number of I/o Port increase in going from lower to higher family member

Increasing memory sizes

The size of main memory increases is going from lower to higher family members.

Increasing Costs.

At a given point in time the cost of a system increases in going from lower to higher family member.

Ans c):-

Stored Program Computers:

A fundamental design approach first implemented in the IAS Computer is known as the Stored Program Concept. this idea is usually attributed to the mathematician John Von Neumann. the first publication of the

Idea was in a 1945 Proposal by Von neumann for a new Computer the EDVAC.

In 1946, Von Naumann and his Colleagues began the design of a new stored. program Computer referred to as the IAS Computer of the princeton Institute for Advanced Studies it Consist of.

A m€s main memory which stores both data and instruction.

An arithmetic and logic unit (ALU) Capables of operating on binary data.

Ans 03:-

Moore's law:-

the famous moore's law which was Proposed by Gordon moore's Co-funder of Intel. In 1965 Moore observed that the number of transistor that Could be put on a single chip was doubling every year and Correctly predicted that this PACE would Continue into the near future.

The Consequences of moore's law are.

1) The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2) The Computer becomes smaller, making it more convenient to Place in a variety of environments.
3) There is a reduction in Power requirements.
4) The interconnection on the integrated circuit are much more reliable than Solder Connection.

Ans E):-

Instruction Cycle State Diagram.

The States in instruction cycle state diagram are follows

Instruction address Calculation:-

Determine the address of the next instruction to be executed.

Instruction fetch:-

Read instruction from it memory location into the Processor.

Instruction operation decoding:
Analyze instruction to determine type of operation to be Performed and operand to be used.

Operand address Calculation:-
If the operation include reference to an operand in memory or available via I/O then determine the address of the operand.

Operand fetch:-
Fetch the operand from memory or read it in from I/O.

Data operand:-
Perform the operation indicated in the instruction.

Operand Stores-
Write the result into memory or out to I/O.

Ans F):-
Classes of Interrupt:
Program:-
It is generated by some condition that occurs as a result of an instruction execution. Such as arithmetic overflow, division by zero

Attempt to execute an illegal machine instruction, or reference outside a user allowed memory space.

Timer:-
It is generated by a timer within the processor that allows the operating system to perform certain function on a regular basis

I/O:-
It is generated by I/O Controller, to signal normal completion of an operation request service from the Processor or to signal a variety of error condition.

Hardware failure:
It is generated by a failure such as Power failure or memory parity error.

Ans 6):-

BUS Interconnection Scheme:
The most Common Computer interconnection structure are based on the use of one or more system bus

A System bus consist typically of about fifty to hundreds of separate lines the lines can be classified into the function groups data address and control lines.

Data line:-

The data line provide a path for moving data among system modules. These lines, collectively are called the data bus.

The data bus may consist of 32, 64, 128, 256, or even more separate lines, the number of lines being referred to as width of data bus.

Address Lines:-

The address line are used to designate the source or destination of the data on the data bus. the width of the address bus determines the maximum possible memory capacity of the system.

Control Line:-

The Control Line are used to control the access to and the use of the data and address line. because the data and address lines are shared by all components.

Typically control line include memory write, memory read, I/O write I/O read reset etc.

Q3
Ans:-
A) Computer Architecture:-

Computer Architecture refers to those attribute of a system visible to a programmer or put another way those attribute that have a direct impact on the logical execution of a program. A term that is often used interchangable with Computer architecture is instruction set architecture.

Computer Organization:-

Computer organization refers to the operation units and their interconnection that realize the architecture specification.
Examples:-

Architectur attributes include the instruction set, the number of bits used to represent various data types (eg numbers, characters).

Ans B):

CISC:-

The Current x86 offering represents the result of decades of design effort on Complex instruction set.

Computer (CISC):-

The x86 incorporates the sophisticated design principle once found only on mainframes and Super Computer and serve as an excellent example of CISC design.

RISC:-

An alternative approach to processor design is the reduced instruction set Computer.

Ans C):-

Microprocessors:

A microprocessor chip include register, an ALU, and some sort of Control unit or instruction Processing Logic. As transistor density increased, it became possible to increase the complexity of the instruction set architecture, and ultimately to add memory and more than one processor. microprocessor chip

Include multiple cores and substantial amount of cache memory.

Microcontrollers:

A microcontroller is a single chip that contains the processor, non-volatile memory for the program (Rom), volatile memory for input and output (RAM), a clock, and an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessor and much higher energy efficiency.

Ans D):-

Cortex-A:

The cortex-A and cortex-A 50 are application processor intended for mobile devices such as smartphone and eBook reader, as well as consumer devices such as digital TV and home gateways e.g. DSL and cable Internet modem.

Cortex-R:

The cortex-R is designed to support real-time

of event needs to be controlled with rapid response to events they can run at a fairly high clock frequency and have very low response latency.

Cortex-M:- Cortex-M series processor have been developed primarily for the microcontroller domain where the need for fast highly deterministic interrupt management is coupled with the desire for extremely low gate count & lowest possible power consumption.

Ans:- E)

In the interrupt cycle, the Processor check to see if any interrupts have occurred indicated by the presence of an interrupt signal.

If no interrupts are pending, the Processor to the fetch cycle and fetches the next instruction of the current Program.

A disabled interrupt simply means that the processor can and will ignore that interrupt occure during the time

it generally remains pending and will ignore that interrupt request signal. If an interrupt remain pending and will be checked by the Processor after the processor has enabled interrupts, when a user program is executing and an interrupt occures, interrupts are disabled immediately.

Nested Interrupt:-

Nested interrupt to allow interrupt of higher priority to cause a lower-priority interrupt handeler to be itself interrupted. A user program begin at t=0. At t=10, a printer interrupt occures user information is placed on the system stack and execution continues at the printer's interrupt service routine. While this routines is still executing at t=15 a communication interrupt occure.

Ans (d):- Programming in Hardware:-

The program is an the form of hardware and is termed as "hardware program

Suppose we construct a general purpose configuration of arithmetic & logic functions. This set of hardware will perform various function on data depending on control signal applied to the hardware. In the original case of customized hardware the system accepts data and produces result

Programming in Software:

The new method of Programming which is a sequence of code and instruction is called Software Programming.

Q4
Ans:- A)

Here is a simple way to understand this problem.
Content are divided up into two 5 bit, instruction, LH & RH

LH instruction = 010FA
opcode = 01
address = 0FA

RH instruction = 210FB
opcode = 21
address = 0FB

Since this is hexadecimal form you have to Converted this number to binary form LH instructions

01 = 0000001 = LOAD m(x)
m(x) refers to the memory address Location 0FA
The first 5 bits of 0BA Should read - LOAD m(0FA)

21 = 0010001 = STOR m(x)
m(x) refers to the memory address location 0FB

The second 5 bit of 0BA Should read - stor m(0FB)
finally the assembly language Code for 0BA 01 0FA 21 0FB is
LOAD m(0FA)
STOR m(0FB)

2: Here is a simple way to understand this Problem.

Content are divide up into two 5 bit instruction LH & RH

LH instruction = 01 0FA
opCode = 01
Address = 0FA

RH instruction = 0f08D
OPcode = 0f
address = 08D
Now convert this number to binary.

LH Instructions

01 = 00000001 = LOAD m(x)
m(x) refers to memory address location 0FA.
The first 8 bits of 08B should read - LOAD m(0FA)

0f = 00001111 = Jump + m(x, 0:19)
refer to memory address location 08D
The second 8 bits of 08B should read - Jump + m(08D, 0:19)
finally the assembly language codes for 08B and 0f08D is.

LOAD m(0FA)
Jump + m(0.8D. 0:19)

3) Here is a simple way to understand this problem.

Contents are divided upto Ist 8 bits instruction LH & RH

LH instruction = 02 0fA
opcode = 02
address = 0fA

RH instruction = 21 0fB
opcode = 21
address = 0fB

Since this is in hexadecimal form you have to convert the number to binary form.

LH Instructions

02 = 00000010 = LOAD - M(n)

M(n) refers to the memory address location 0fA.

The first 8 bit of 0Bc should read - LOAD - M(0fA)

21 = 00100001 = STOR M(n)

M(n) refers to the memory address location 0fB

The second 8 bits of 0Bc should read - STOR M(0fB)

LOAD = M(0fA)
STOR = M(0fB)

Ans c):-

Effective CPI:-

$$CPI = (1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 9000)/100$$

$$CPI = 162000/100$$

$$CPI = 1620$$

$$\text{MIPS rate} = 60\,MHz / 1620 \times 10^6$$

$$\text{MIPS rate} = 60 \times 10^6\,Hz / 1620 \times 10^6$$

$$\text{MIPS rate} = 60\,Hz / 1620$$

$$\text{MIPS rate} = 0.037$$

$$T = I_c / (\text{mips} \times 10^6)$$

$$T = 104000 / (0.037 \times 10^6)$$

$$T = 104000 / 37 \times 10^3$$

$$T = 2811 \times 10^{-3}$$

$$T = 2.811\,sec$$

Ans b):-

In OBA address the m(OFA) transfer to the accumulator & transfer contents of accumulator to memory location OFB.

In OBB address the m(OFA) transfer to the accumulator & take next instruction from left half of m(OBB)

Ans D:-

Since we have the same instruction mix, that means the additional instructions for each task could be allocated appropriately between the instruction types, therefore the following parallelizable is $f=1$ then Amdahl's law decrease to Speedup $N=8$. therefore, the actual speedup is only about 75% of the theoritical Speedup.

Ans E):-

* The PC Contain 300, the address of the first instruction this value is loaded into the MAR.

Ans f):-

2^{24} = 16 mBytes

a) if the local address bus is 32 bits the whole address can be transferred at once and decoded in memory However because the data bus is only 16 bits. it will require 2 cycle to fetch a 32-bit instruction or opereand.

b) A 16 bits of the address on the bus can't the whole memory. Thus a Complex memory interface control is needed to latch the first part of the address and then second part.

c) The Program Counter must be at least 24bits typically 32-bit microprocessor will have a 32 bits external address bus and a 32 bit Program Counter. Unless on chip segment registers are used that may works with a small Program Counter. then it will have to be 8 bits long.

* The value in the MAR is loaded into the IR.
* The address portion of the IR (940) is loaded into the MAR.
* The value in the MBR is loaded into the AC.
* The value in PC (301) is loaded into the MAR.
* The value in the MBR is loaded into the IR.
* The address portion of the IR (941) is loaded into the MAR.
* The value is location ~~into the MAR~~ 941 in loaded into MAR.
* The value in PC (302) is loaded into the MAR.
* The value in the AC is loaded into the MBR.
* The address portion of the IR (941) is loaded into the MAR.

Ans (b):-

A bus cycle takes 0.25 μs, so a memory cycle takes 1 μs. If both operands are even aligned, it take 2 μs to fetch the two operands. If one is odd aligned the time required is 3 μs. If both are odd aligned, the time required is 4 μs.