-: Q1 :-

Part (a)

Word :-

The natural unit of orgnization of memory. The size of word is typically equal to the number of bits used to represent an integer.

Addressable Units :-

In some System. the addressable unit is the word. However, many system allow addressing at the byte level.

Unit of transfer :-

For main memory This is the number of bits read out at or written into memory at a time. The unit of transfer need not equal a word (or) an addressable unit.

:Q1:-

Part (b)

LRU:-

For two-way set associate this is easily implemented. Each line includes a use bit, when a line is referenced, its use bit is set to 1 and the use bit of the other line in that set to 0. when a block is to be read into the set the line whose USE bit is 0 is used.

LFU:-

LFU could be implemented by associating a counter with each line. A technique not based on usage is to pick a line at random from among the candidate lines

-:Q1:-

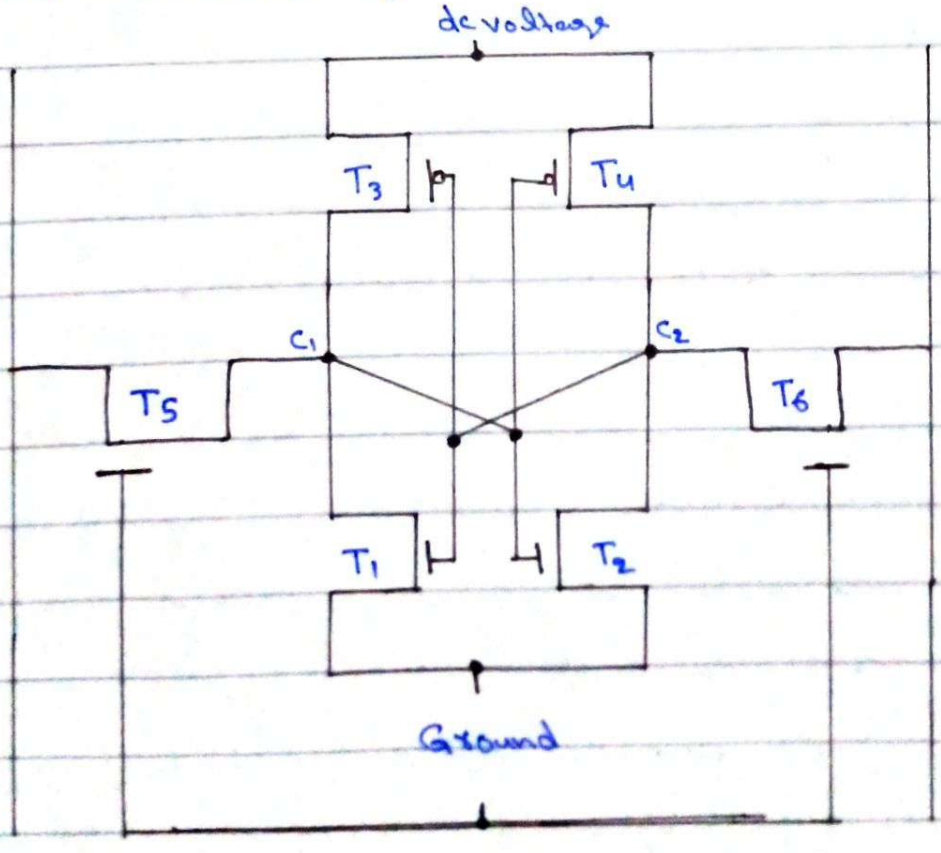
Part (C)

Read operation :-

in SRAM for any operation to be performed the word line should be high To perform read operation, initially.

Write operation :-

Consider the memory bits consists of Q = 0 and Q' = 1



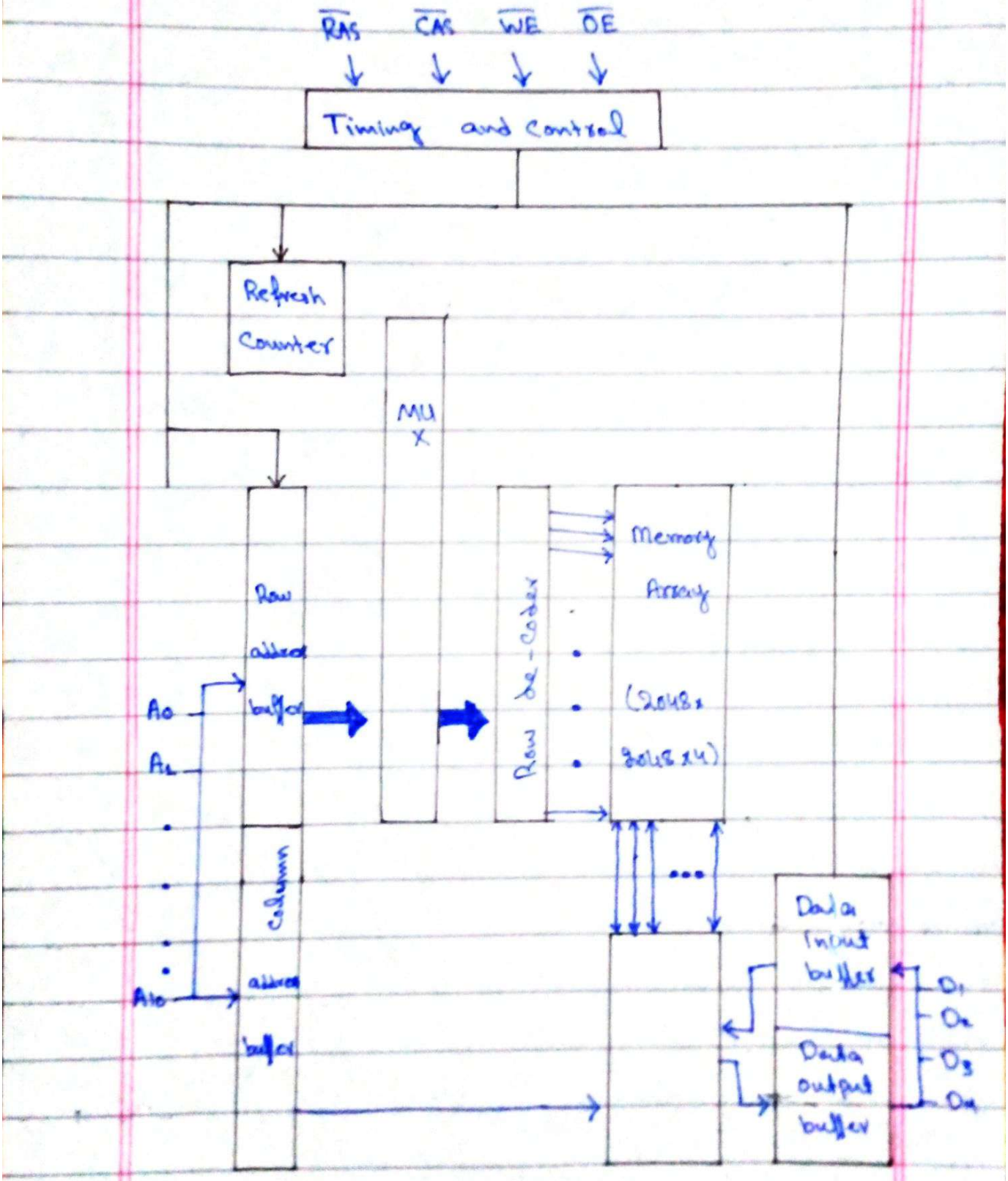
-: Q1 :-

Part (d)

16-Mbit DRAM :-

In this case 4-bits are reads or written at a time. Logically the memory array is organized as four square arrays of 2048 by 2048 elements. Various physical arrangements are possible. In any case, the elements of the array are connected by both horizontal and vertical lines. Each horizontal line connects to the select line terminal of each cell in its row; each vertical lines connects to the Data-In/Sense terminal of each cell in its column. Because only 4 bits are read/written to this DRAM, There must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

Diagram:-


RAS
CAS
WE
OE
Timing and control
Refresh Counter
MUX
Row address buffer
Row decoder
Memory Array
(2048 x 2048 x 4)
Column address buffer
Data input buffer
Data output buffer
A0
A1
A10
D1
D2
D3
D4

-:Q1:-

Part (e)

Reasons :-

The DVD's greater capacity is due to three difference from CDs

⇒ Bits are packet more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm.

⇒ The DVD employs a second layer of pits and lands on top of the first layer. A dual-layer DVD has a semireflective layer on top of the reflective layer and by adjusting focus, the lasers in DVD drives can read each layer separately

⇒ The DVD-ROM can be two sided. where as data are recorded in only one side at a CD. This leads total capacity upto 17GB.

-:Q2:-

Part (a)

EEPROM :-

Electrically erasable programmable read-only memory (EEPROM) is a read-mostly memory that can be written into at any time without erasing prior contents only the byte or bytes addressed are updated. The write operation takes considerably longer than the read operation. EEPROM is more expensive than operation. EEPROM is more ~~it~~ expensive than EPROM and also is less dense, supporting fewer bits per chip.

Flash memory :-

Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few second which is much faster than EPROM Flash memory does not provide byte-level

erasure

-:Q2:-

Part (b)

Hard Failure:-

A hard failure is a parmanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 (or) 1 (or) switch erratically between 0 & 1.

Hard errors can be caused by harsh envirement abuse, manufacture defects & wear.

Soft w error:-

A soft error is a random nondestructive event that alters the contents & one or more memory cells without damaging the memory.

Soft errors can be caused by power supply problems or alpha particles. Both hard and soft errors are clearly undesirable.

-:Q2:-

Part (c)

Magnetic Disk

Read Mechanisum:-

The traditional read mechanism exploits the fact that a magnetic field moving relative to a will produces an electrical current in the coil. when the surface of the disk rotates under the head, it generate a current of the same polarity as the one already recorded.

Write Mechanism:-

The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field. Electric pulses are sent to the write head, and the resulting magnetic patterns are recorded on the surface below, with different patterns for positive and negative currents.

-: Q2 :-

Part (d)

Parallel Access :-

All member disks are Participate in the execution of every I/O request. Typically, the spindles of the individual drives are synchronized. So that each disk head in the same position on each disk at any given time.

Independent Access :-

Each member disk operates independently. so that seperate I/O requests can be satisfied in parallel.

-:Q2:-

Part (e)

HD DVD :-

The HD DVD scheme can store 15GB on a single layer on a single side.
HD dvd players have been much cheaper than Blu-ray machines.
It deliver sharp resolution.
It is a cheaper than Blu-ray.

Blu-ray DVD :-

Blu-ray discs have more storage space and more advanced protections against piracy
It also deliver sharp resolution
Blu-ray has 25GB capacity and is more expensive than HD dvd.

-: Q3 :-

Part (a)

Memory access methods

Sequential Access:-

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single Linked list. The access time depends on the location & the data. Applications & the sequential memory access are magnetic tapes, magnetic disk and optical memories.

Random Access:-

In this methods, any location & the memory can be accessed randomly like accessing in Array. Physical location are independent in this access methods Application are & this random memory access are- RAM and ROM.

Direct Access:-

In this method, the particular location & the memory can be accessed directly like accessing in Array. This method is a combination & above two access methods. The access time depends on both the memory organization and characteristics & storage technology the access is semi-random or direct Application & this direct memory is magnetic hard disk.

Associate Access:-

In this memory word is accessed rather than its address. This access method is a special type & random access method Application & this direct memory access is Cache memory.

-:Q 3:-

Part (B)

Principle of Locality:-

The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

(OR)

An implication of locality is that we can predict with reasonable accuracy what instruction and data a program will use in the near future based on its accesses in the recent past.

-:Q3:-

Part (c)

Possible approaches to cache coherency

Bus watching with write through:-

Each cache controller monitors the address lines to detect write operations to memory by other bus master. If another master writes to a location in shared memory that also resides in the cache memory the cache controller invalidates that cache entry. This strategy depends on the use of a write-through policy by all cache controllers.

Hardware transparency:-

Additional hardware is used to ensure that all updates to main memory via cache are reflected in all caches. Thus, if one processor modifies a word in its cache this update is written to main memory. In addition, any matching words in other caches are similarly updated.

non-cacheable memory:-

Only aportion of main memory is shared by more than one processor, and this is designated as non-cacheable. In such a system all accesses to shared memory are cache misses, because the shared memory is never copied into the cache. The non-cacheable memory can be identified using chip-select logic or high-address bits.

-: Q3 :-

Part (D)

Practical Issues peculiar to SSDs

⇒ SDD Performance has a tendency to slow down as the device is used :-

- The entire block must be read from the flash memory and placed in a RAM.
- Before the block can be written back to flash memory the entire block of flash memory must be erased.

- The entire block from the buffer is now written back to the flash memory.

⇒ Flash memory becomes unusable after acertain number of writes:-

- Techniques for prolonging life:

- Front-ending the flash with a cache to delay and group write operations.

- Using wear-leveling algorithms that evenly distribute writes across block & cells.

- Bad-block management techniques.

- Most flash devices estimate their own remaining lifetimes. So system can anticipate failure and taker preemptive action.

-:Q3:-

Part (E)

CD read operation:-

Information is retrived from a CD (or) CD-ROM by a low-powered laser housed in an optical-disk player (or) drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounter a pit. Specifically, if the laser beam falls on pit, which has a some what rough surface, the light scatters and a low intensity is reflected back to the source. The area between pits are called lands. A land is a smooth surface, which reflects back at higher intensity. The change between pits and lands is detected by a photo sensor and converted into a digital signal. The sensor tests the surface at regular intervals. The beginning

end & pit represent a '1', when no change in elevation occurs between intervals, a 0 is recorded.

CD write operation :-

Recall that on magnetic disk, information is recorded in concentric tracks. with the simplest constant angular velocity (CAV) system, the number of bits per track is constant An increase in density is achieved with multiple zoned recording, in which the surface is divided into a number of zones, with zones farther from the center containing more bits than zones closer to the center. Although this technique increases capacity it is still not optimal.

∴ Q4:-

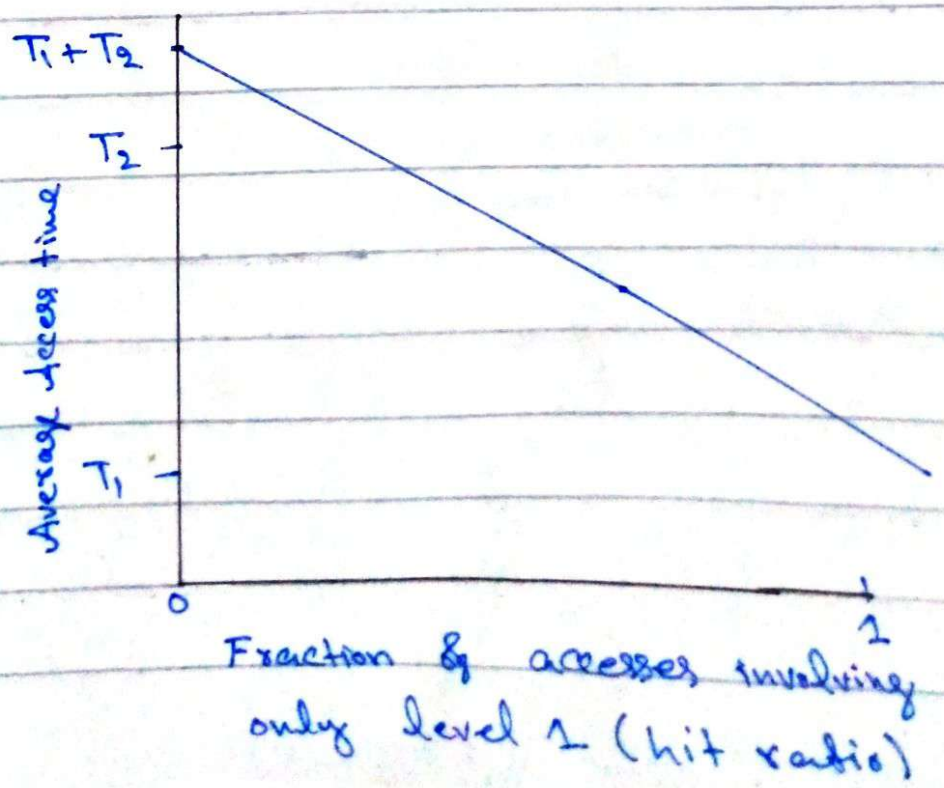
Part (a)

In example, suppose 95% of the memory access are found in level 1. Then the average time to access a word can be expressed as

$$(0.95)(0.01\,\mu s) + (0.05)(0.01\,\mu s + 0.1\,\mu s)$$
$$= 0.0095 + 0.0055$$
$$= 0.015\,\mu s$$

The average access time is much closer time ~~is~~ to 0.01μs than 0.1μs as desired.

Curve:-



-: Q4 :-

Part (b)

Main memory address = 9F3A7Ch

in binary

100111110011101010111001100

Tag	Set	Word
10011111	0011101011100	11
← 9 bits →	← 13 bits →	← 2 bits

Part (c)

$m = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
X	0	1	X	1	0	0	X	0	0	1	0

bits are in bit number 1, 2, 4, and 8

Check bit 8 Calculated by values in bit number 9, 10, 11 and 17

Check bit 4 Calculated by values in bit number 5, 6, 7, and 12

Check 1 bit calculated by value in bit number 3, 5, 7, 9 10 and 11

Thus the check bits are

1011

Ans part (d)

(1) Average Seek = 6 ms

Average rotational delay = 3 ms

Read 500 Sectors = $\frac{6ms}{15ms}$

Total time = 15 + (6 x 7)

= 15 + 42

= 57

=

0.057 sec

(2) Average seek = 6ms

Rotational dely = 3ms

Read 1 sector = 0.012 ms / 0.012ms

Total time = 2500 × 9.012

= 22530ms

= 22.53 seconds.

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Subject/paper :- Computer Architecture.