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SUBJECT: DIGITAL LOGIC DESIGN

SEMESTER: 3<sup>RD</sup>

**PROGRAMME:** BS (SOFTWARE ENGINEERING)

Date: .....

Q1) Draw and explain logic ----?

a) A circuit for adding or sub----

1) Full adder:

The full adder is logical circuit that perform an addition operation on three binary digits and one just on half adder it also generate carry

A →	4 bit full adder	sum	Cin
B →		→	A
C →		carry	B
Cin →		→	C

b) 4 bit full subtractor

The 4 bit full subtractor is logical circuit, that perform subtractational operation on three binary digits and just like on half subtractor it also generate borrow in many ways full subtractor can be used as

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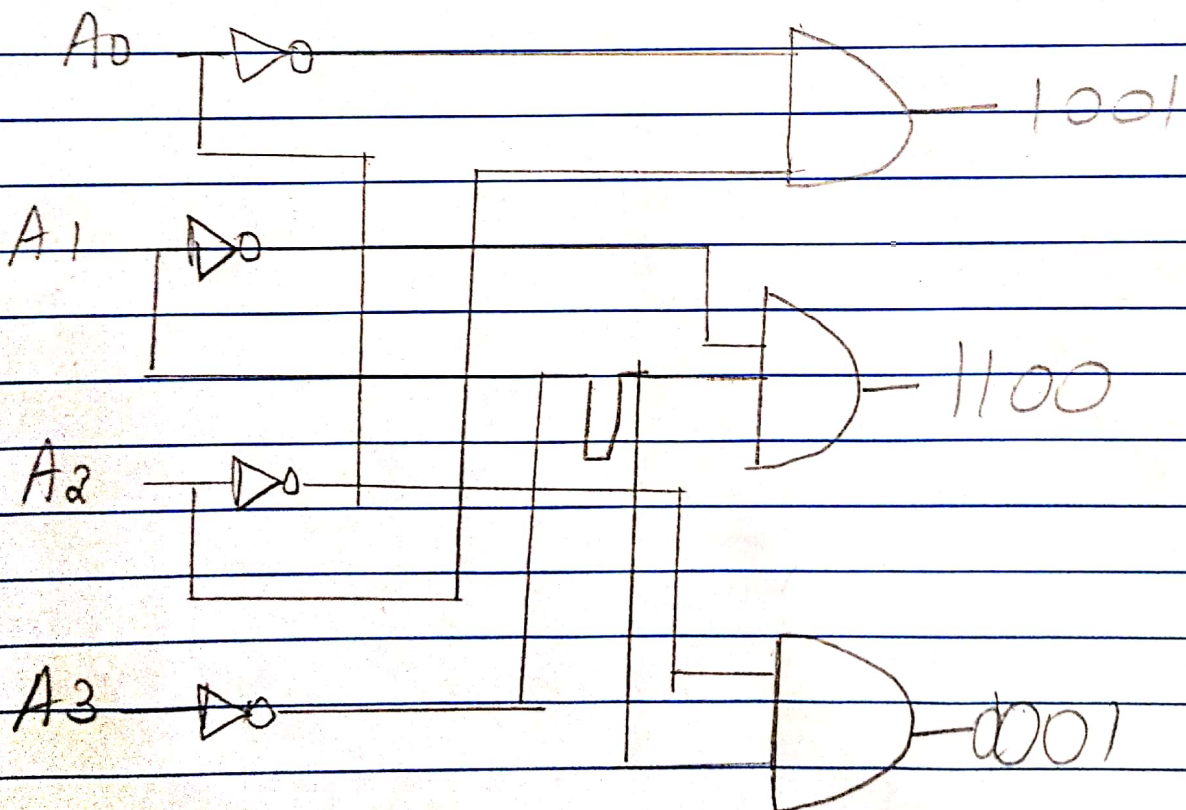


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half subtractor connected together.

A	4 bit full subtractor	→ Difference
B		
C		→ Borrow
B <sub>m</sub>		

6 4 bit active low decoders



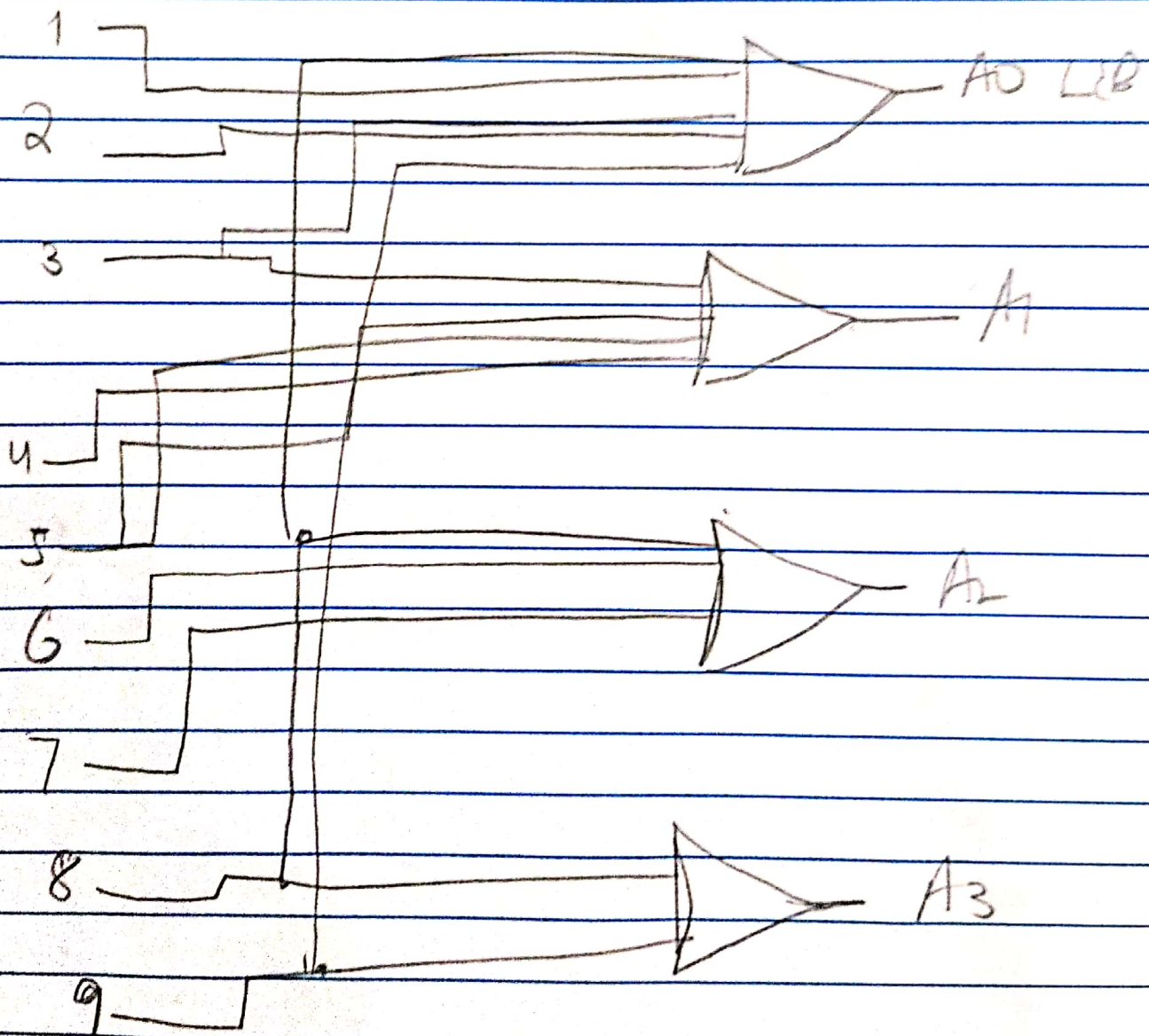
Here we used 4, 6 & 8 input signal  
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and it detects the value 1001  
The active low decoder means that  
output is active it has logic  
value which is low

### c) Decoded to BCD decoder:



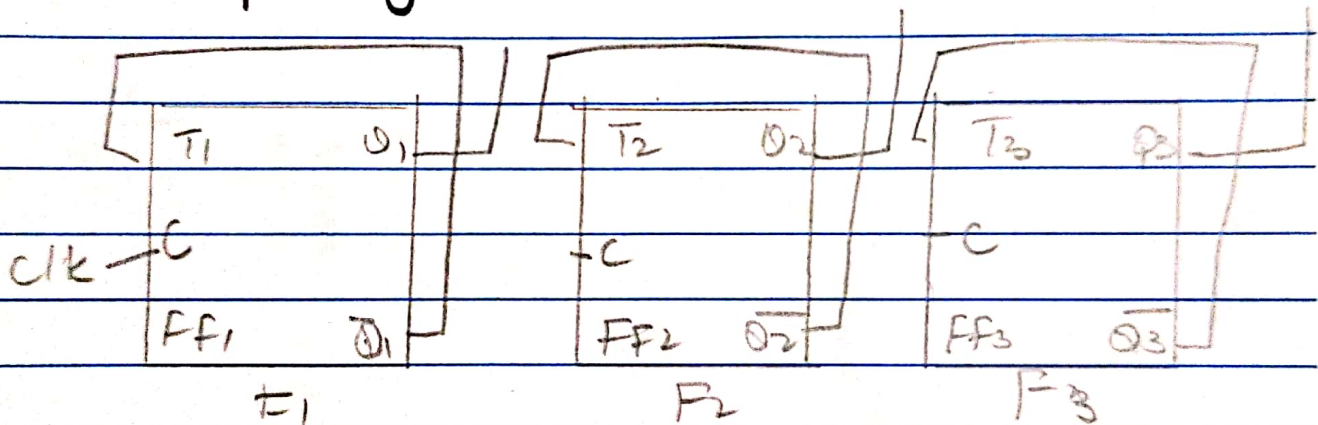
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A decimal to BCD encoder is also known as 10 line to 4 line encoder. It accepts 10 inputs and produces 4-bit output corresponding to each decimal input.

d) Frequency divide - - - - ?



Here we assume the frequency is 16 kHz

$$\text{so } f/2, \quad f = 16/2 \\ f = 8 \text{ kHz}$$

Q2) For 4 input - - - - ?

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a)  $S_0 = 1$

$S_0 = 1$

$S_1 = 0$

$D_0 = 0$

$D_1 = 1$

$D_2 = 0$

$D_3 = 1$

$D_0 = 1$

y

$S_0 \cdot S_1 = 10 \Delta 0$

b)  $S_0 = 0, S_1 = 1$

$S_0 = 0$

$S_1 = 1$

$D_0 = 0$

$D_1 = 1$

$D_2 = 0$

$D_3 = 1$

$D_1$

$S_0 \cdot S_1 = D_1$

0.1

c)  $S_0 = 1, S_1 = 1$

$S_0 = 1$

$S_1 = 1$

$D_0 = \text{---}$

$D_1 = \text{---}$

$D_2 = \text{---}$

$D_3 = \text{---}$

$D_1 \times$

$S_0 = S_1 = D_1$

1.0

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d)  $S_0 = 0, S_1 = 0$

$S_0 = 0$	
$S_1 = 0$	
$D_0 = 0$	
$D_1 = 1$	$D_3$
$D_2 = 0$	$\rightarrow S_0 \cdot S_1 = D_3$
$D_3 = 1$	1-1



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# Q3 Timing diagram -----?

Even

Odd

A<sub>0</sub>

A<sub>1</sub>

A<sub>2</sub>

A<sub>3</sub>

A<sub>4</sub>

A<sub>5</sub>

~~A<sub>7</sub>~~

~~A<sub>6</sub>~~

Even

-1

-2

-3

-4

-5

-6

-7

-8

-9

-10

-11

-12

-13

-14

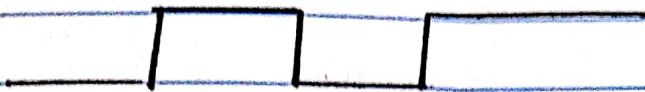
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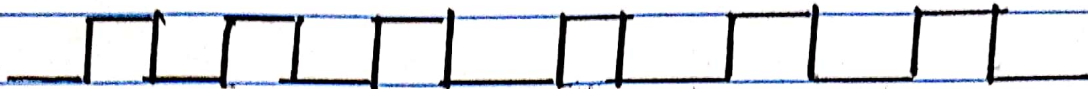
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Q<sub>old</sub>



(Q<sub>y</sub>)

CLK



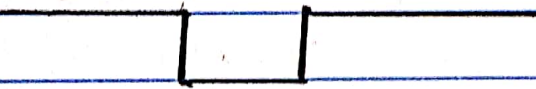
J



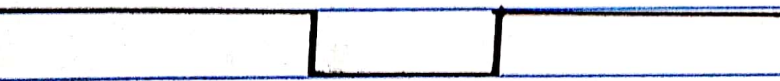
K



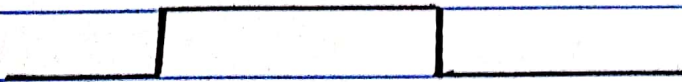
PRE



$\overline{CLR}$



Q

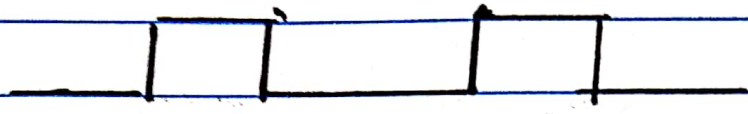


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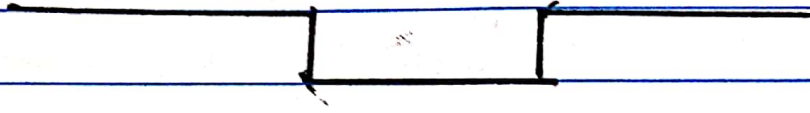
CLK



D = 1:



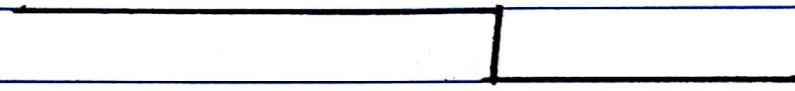
Q0



Q1



Q2



Q3

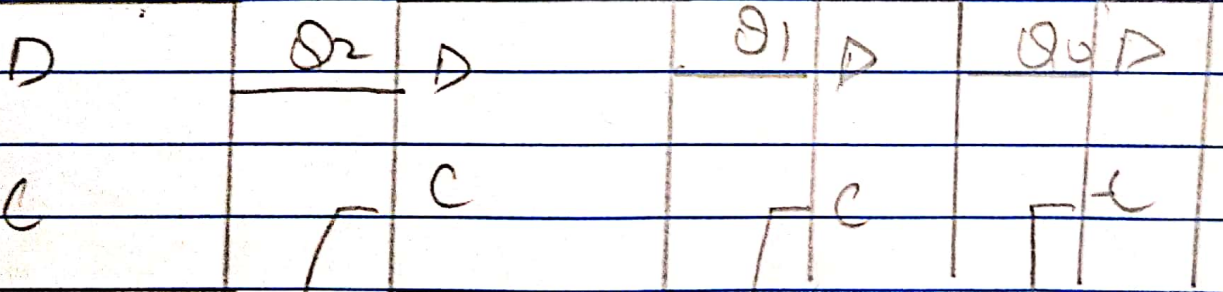


FF0

FF1

FF2

FF3



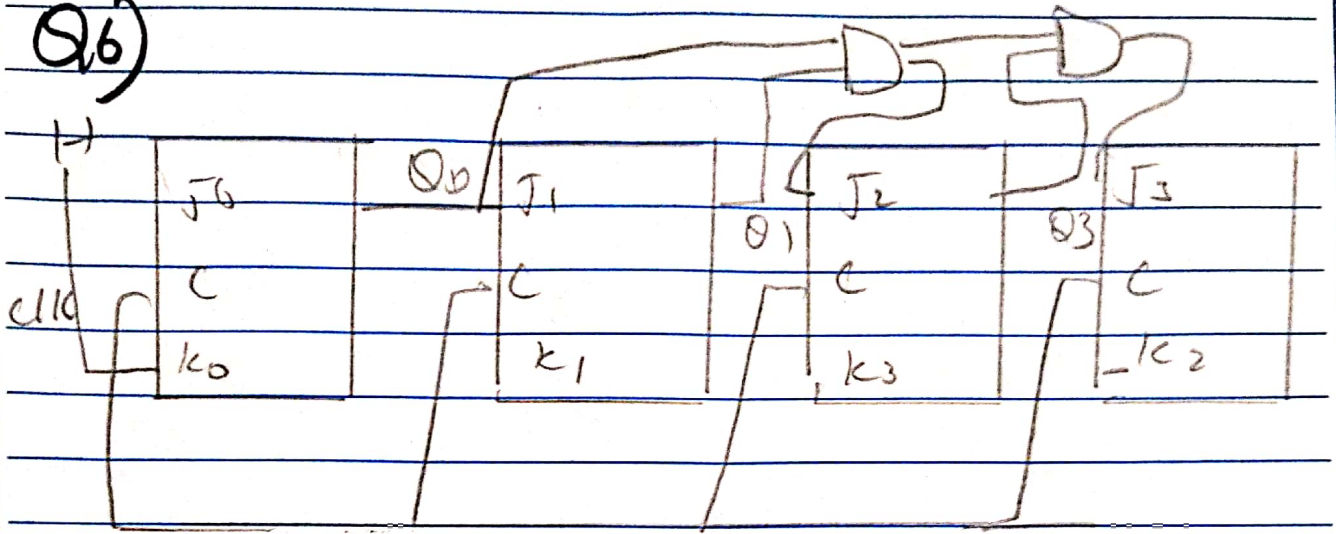
CLK

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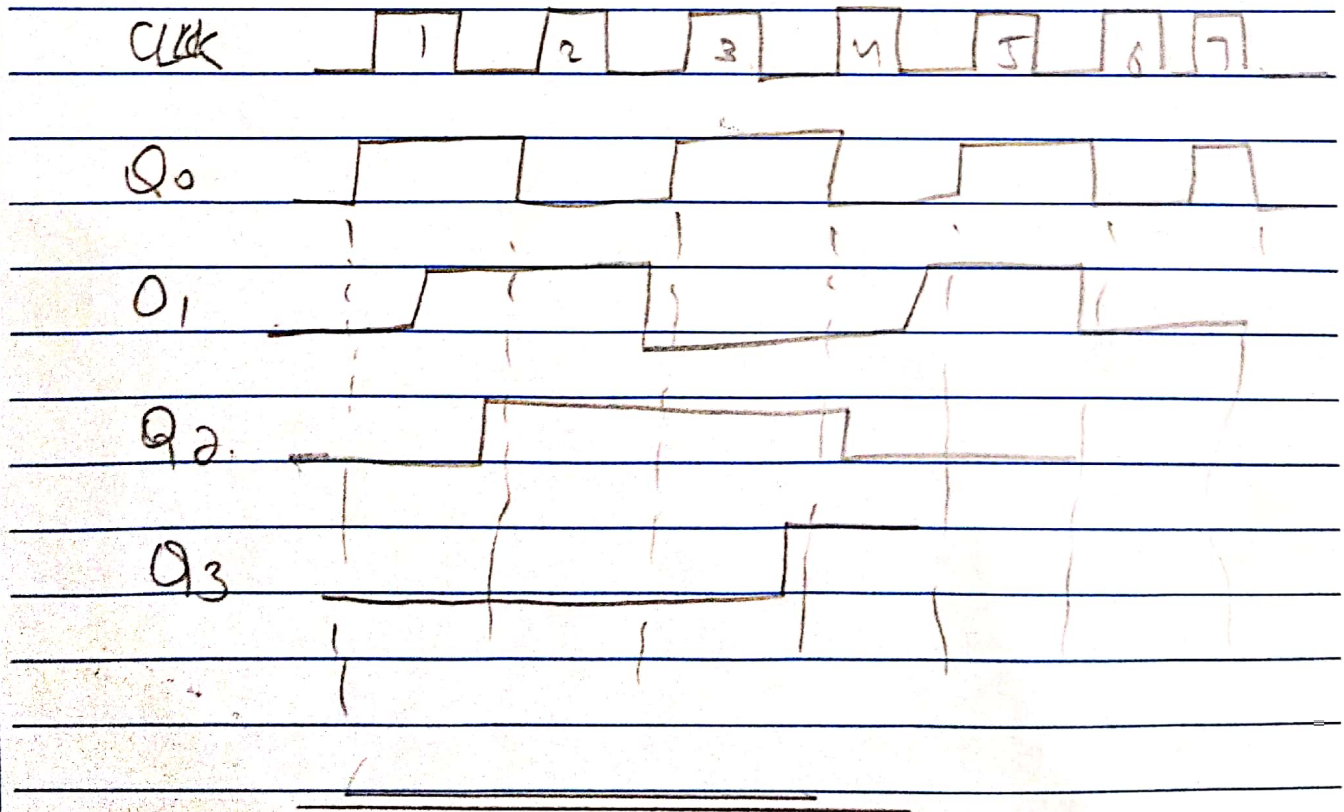


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Q6)



P.J.O



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