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SUBJECT: DIGITAL LOGIC DESIGN

SEMESTER: 3RD

PROGRAMME: BS (SOFTWARE ENGINEERING)

Date: Q1) Draw and emphasin logic ---? a) A circuit for adding or Sb----? i. C Full adder: ŝ The full adder rs logical circuit hat perform an addition operation on three bhary digits onel ore just on helf addord it also generate circy S A --> sum 4 bit full 200 adder awry Cin -> 4 bit Jule Subtractor 6.7 4 The 4 bit Jul Jubbractor is Logical circuit, That S perform subtractional operation on three bhary digits and just like on half subtractor It also generate borrow in many ways jul subtractor can be used as 6 APM A Sa

Date: N La subtractor Connected together. half 200 bit Jul A 4 C Ć subtraction 3 Bin bit active decodesa Low b Aa E La Aere 4 land we used sagne J. APM (Sav) Va So C 4.6 3

74 A Date: and it detects the value 1001 10.200 • The active low decoder meens meet S value. which is low . c) Resment to BCD ecoder: 1 X 3 3 D. y 2 S いう • 8 3 0 E \mathcal{APM}

Date: is also A decimal to BCD encodes 10 line to 4 line encoder known as 10 mput and product 45A accepts 5f output corresponding inpu decine divide reguence 2 0, 02 TI 12 20 +C cik Ff, FFL FF3 D 02 03 120 Fr モー S Here assume me 16 KHz are rs requerey 80 16/2 8/CHZ 2 2 08 Input APM

a) So=1			
8=1			
Do O			
D_2		D = 1 y	
DJ		So	.JI = 10 DO
b $c_{0} = 0$			
b) SO=D, SI	= /		
80 = 0		2	
$\frac{l=1}{DOD}$			
	2		0 · JI = D.
D2 D3			0.1
0) So=1. Si.	= 1	r	
	soel		
	3121		Dr.
	Do		V

Date:

d) $So = O$, $S_{1} = D$	
10 = 0	
S_{1z}	
Do = O	
$D_{1=1}$	DS
D2 2D	- Y SO 5 = D3
$D_2 = D$ $D_3 = L$	1.)
	9520 9
상 4월 19일 전 1월 20일 전 1 1월 20일 전 1월 2	
	· · · · · · · · · · · · · · · · · · ·
	APM

OB Timing dragram?	
even	
	-1
Odd	-2
AO TIT	- 3
	-4
H1	-5
A2	-6
A3	
	+
Ay	
As	-93
A4	
A6	
Even	

Date:	
odd	
QY)	
CIK	
J TITL	1
K IIII	
PRE	
CLE	
9	<u></u>
	(
AP	

CLK			
D = 1=			
Qo			
QI		*.	
Q 2		1	
Qs			-
PPO	FFI	FF2 1 OID	FF3
lk			
			APM

Sa ell 1 20 1 Date: 10 26 S 2 Ob 7 0 03 C ald • • A Real K1 1C2 ko k3 S P 0 • 7 \$ CLER 5 1 2 3 M Â Qo 26 1 1 0, (0 Ì 9 2 200 ----S 0 2 2 C 4 APM 10.4