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ID: 15478

SUBJECT: DIGITAL LOGIC DESIGN

SEMESTER: 3<sup>RD</sup>

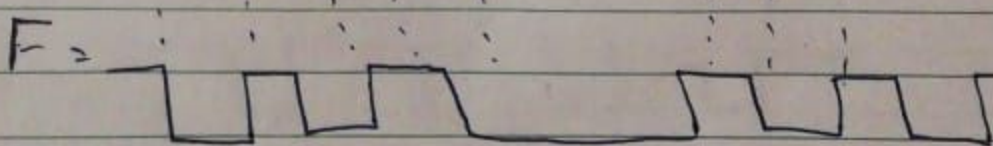
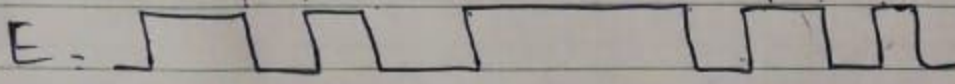
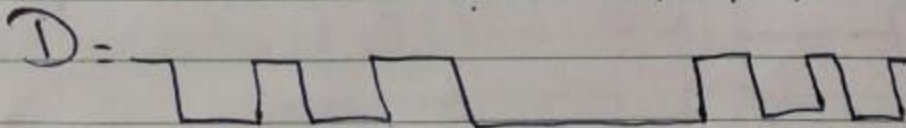
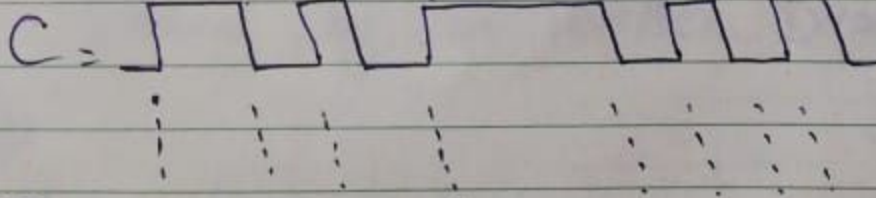
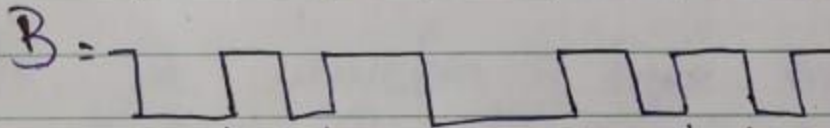
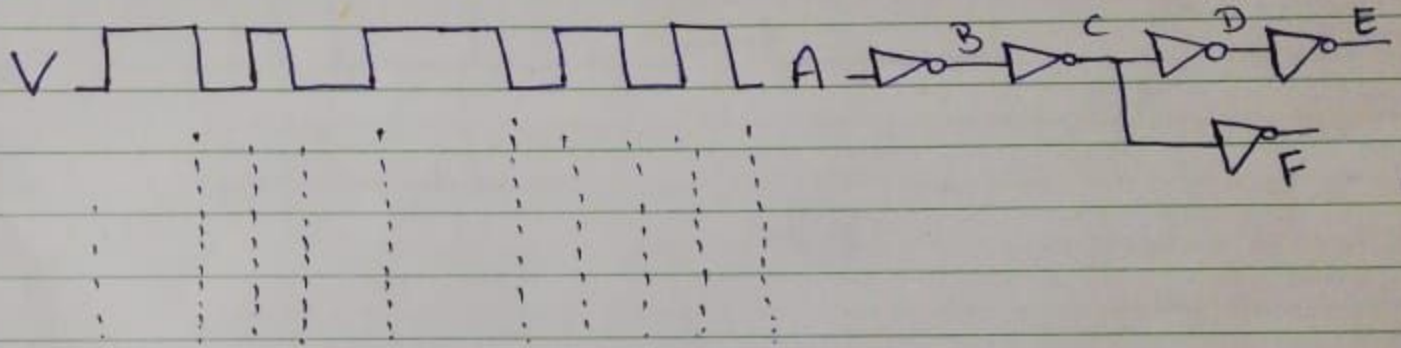
**PROGRAMME:** BS (SOFTWARE ENGINEERING)



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Q3: If waveform in  $Q_1$  is applied to figure in  $Q_2$  at point A. Determine the waveform from point B to F.

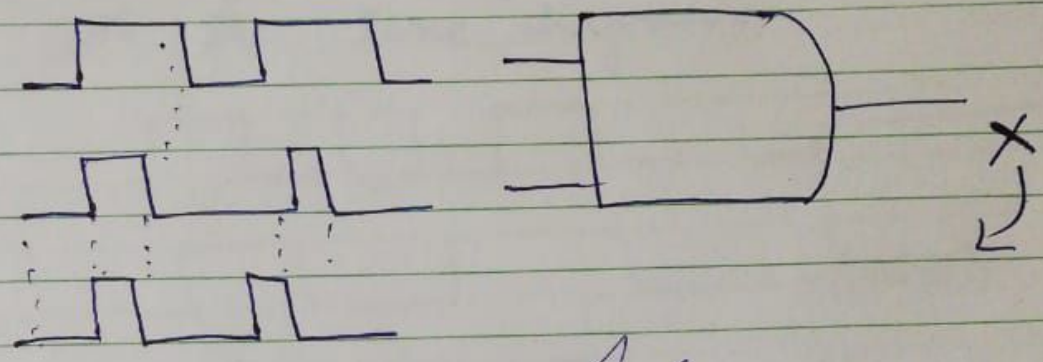
Sol



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Q4: Determine the output, X for a 2input AND gate with the input waveform in figure.

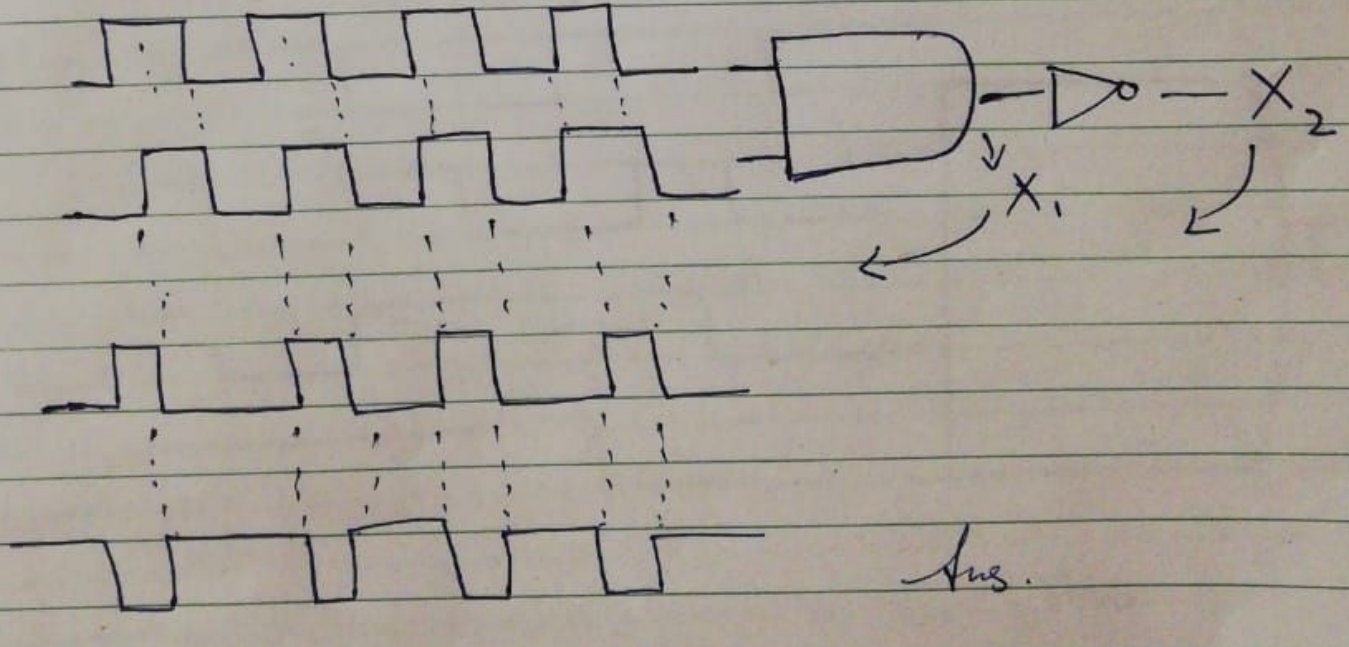
Sol



Ans:

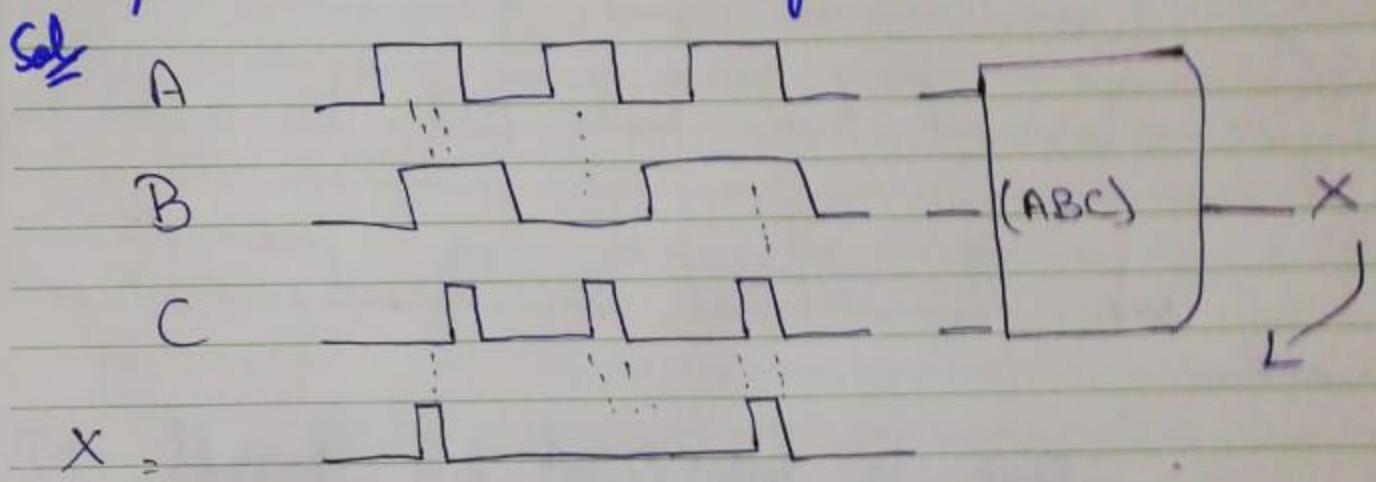
Q5: The waveform in figure are applied to point A and B of a 2input and gate followed by an inverter. Draw the output waveform

Sol

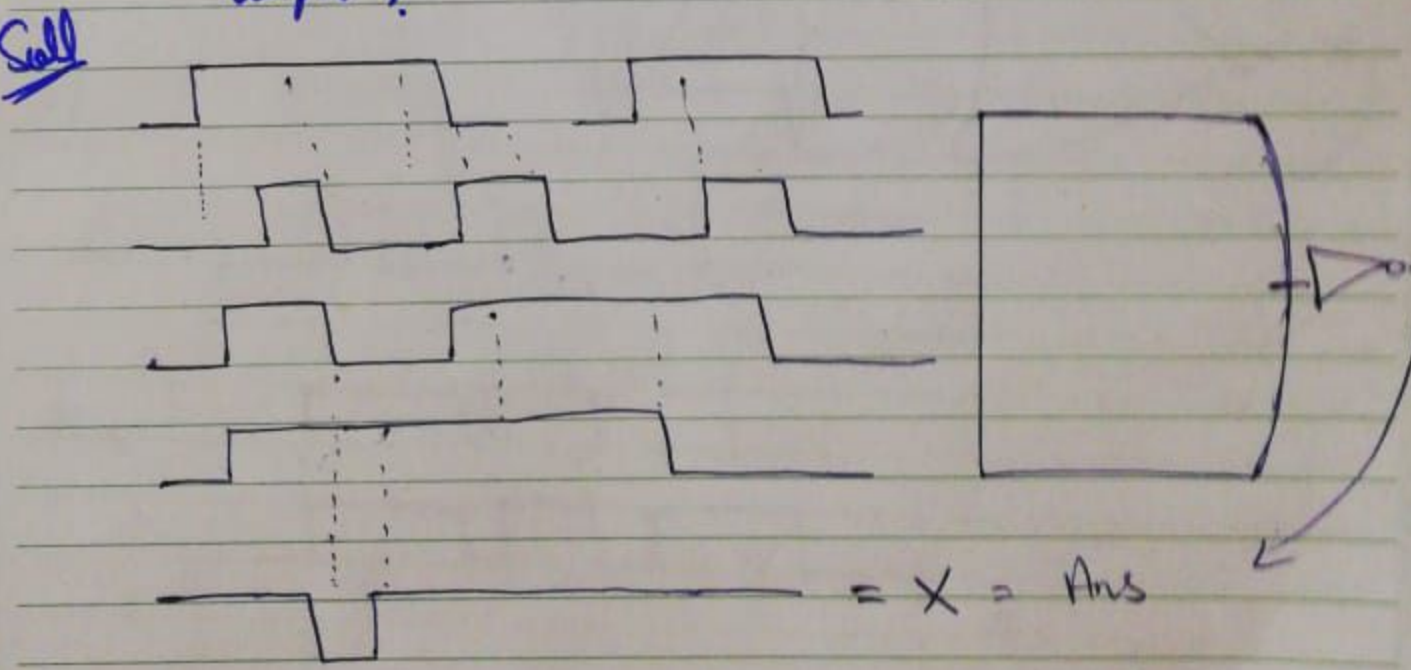


Ans.

Q6: The input waveform applied to 2-input and gate one of indicated in figure show the output waveform in proper relation to the input with the time diagram.

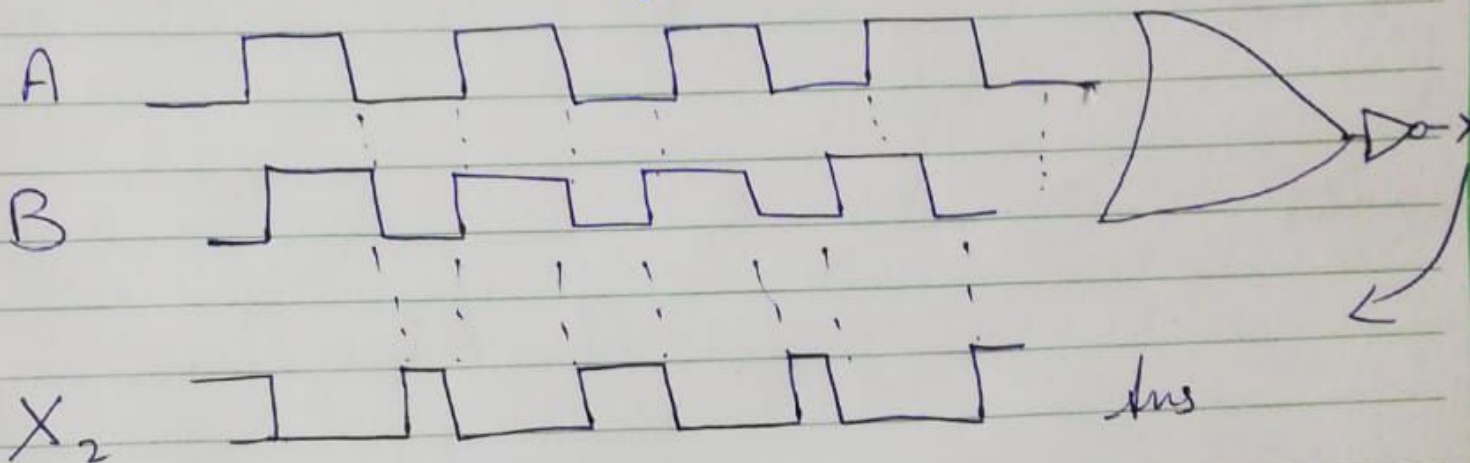


Q7: The input applied to a 4 input AND gate as indicated in figure. The output is fed to inverter. Draw the not output?

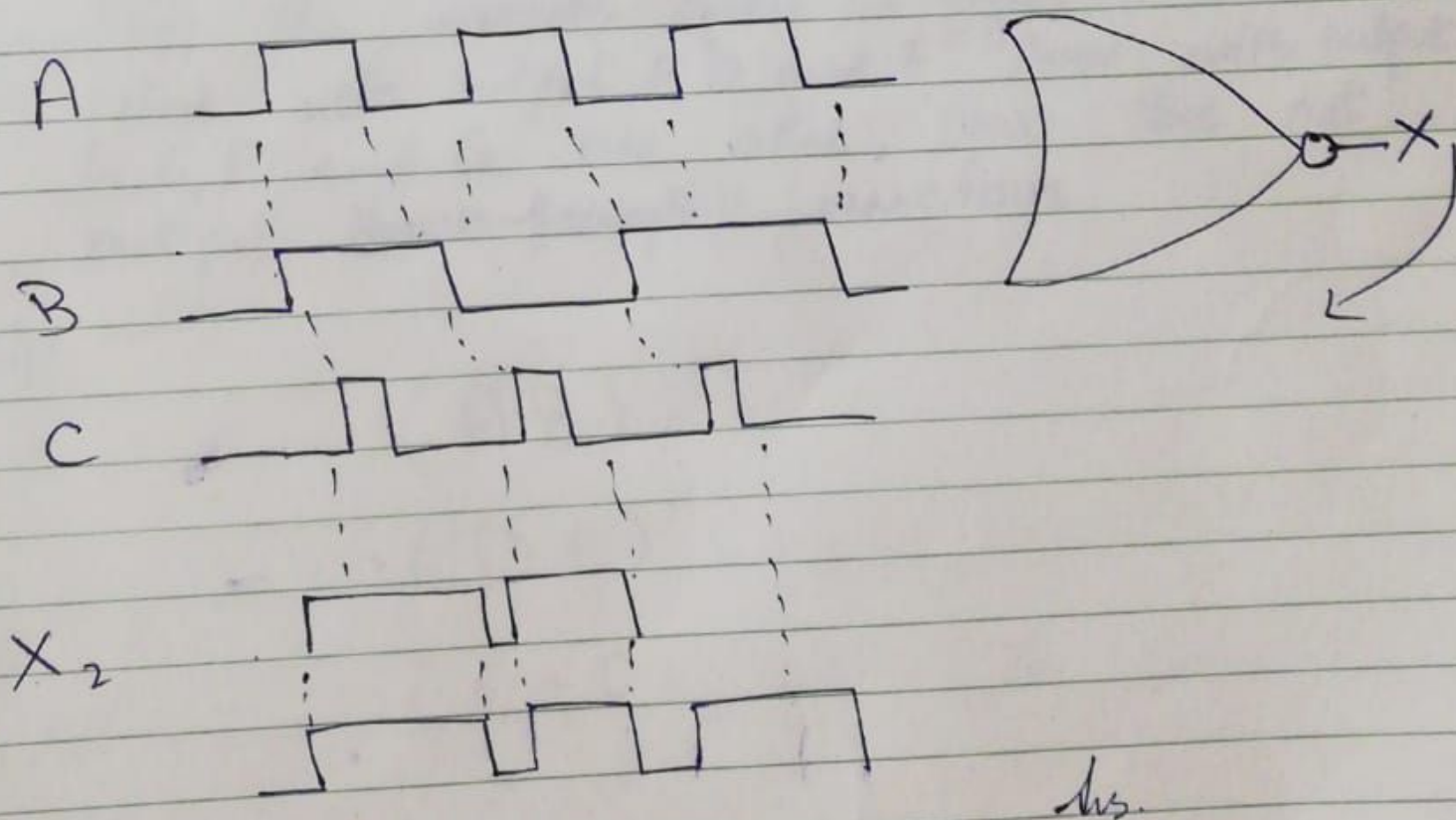


Q8: Determine the output for a two input OR gate when input waveform are as in figure Q5. and draw a time diagram.

Sol



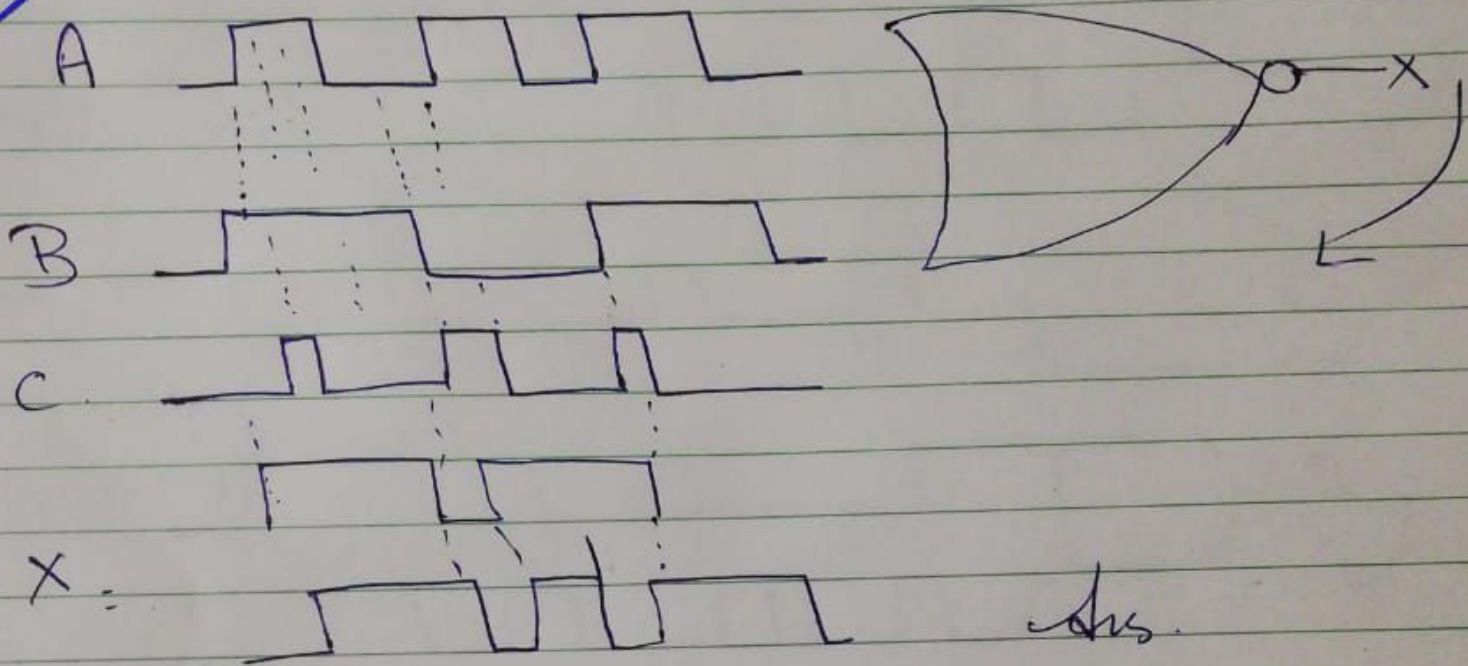
Q9: Repeat Q.6 for 3 input OR gate.



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Q10: Repeat Q7 for 4 input OR gate.

sol



Q11: For the waveform given in figure, A and B are ANDed with output, F, D and E are ANDed with output G, C, F and G are ORed, Draw the net output waveform.

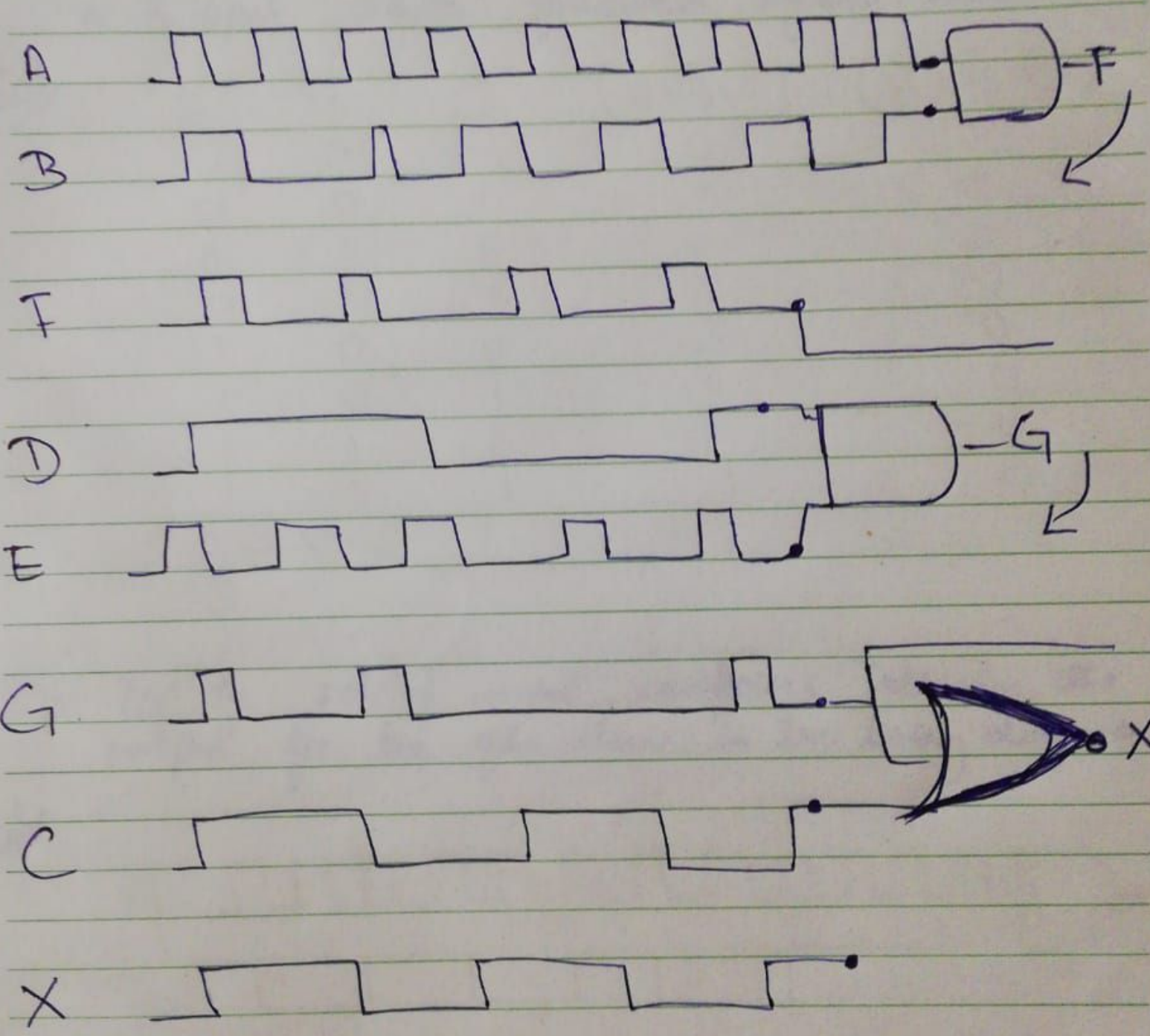
sol

$$(A \cdot B) = F$$

$$(D \cdot E) = G$$

$$(C + F + G) = X$$

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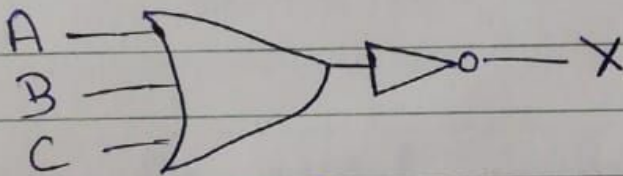


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Q12: Show the truth table for a system of a 3 input or gate followed by an inverter.

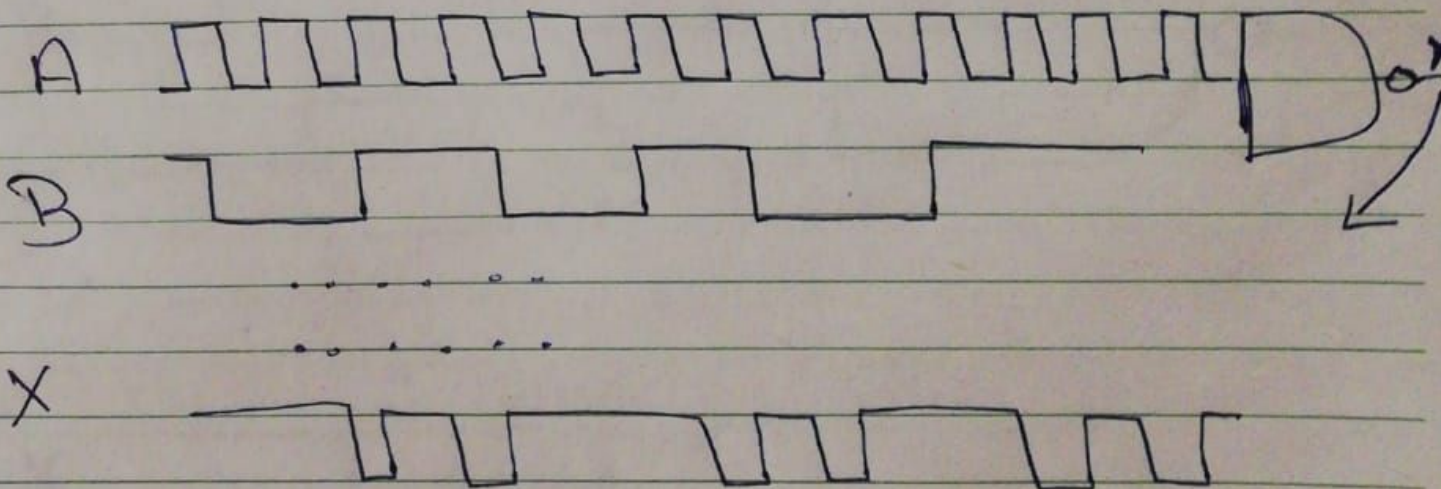
Sol

A	B	C	$(A+B+C)$	$\neg(A+B+C)$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0



Q13: For the set of input waveforms, Determine the output for the gate shown in the timing diagram.

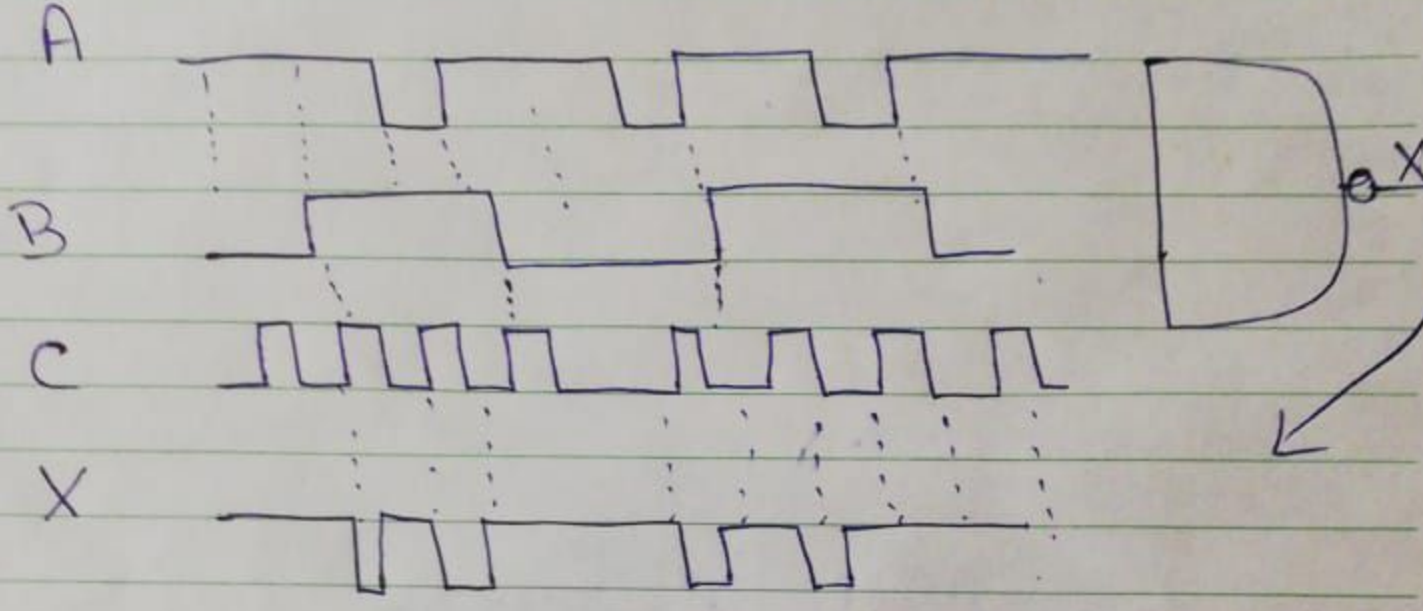
Sol



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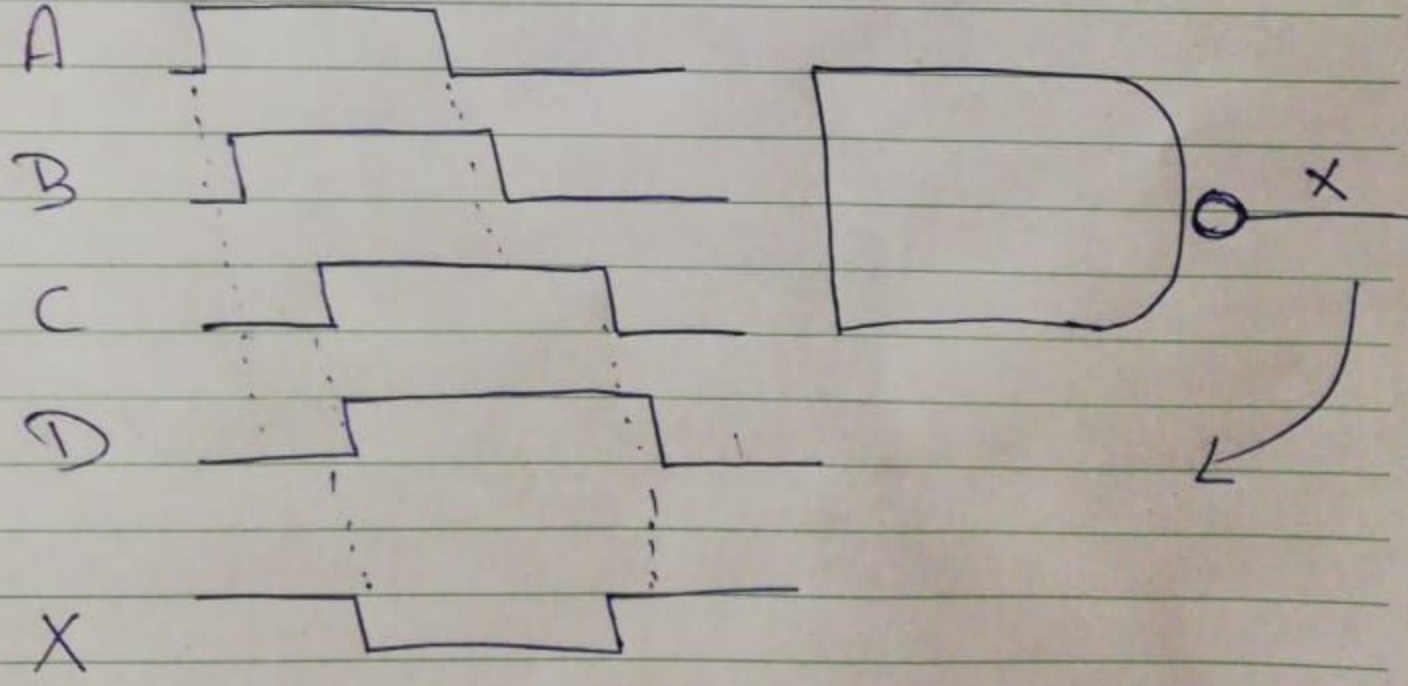
Q14: Determine the gate output for the input waveforms in figure and draw the timing diagram.

Sol



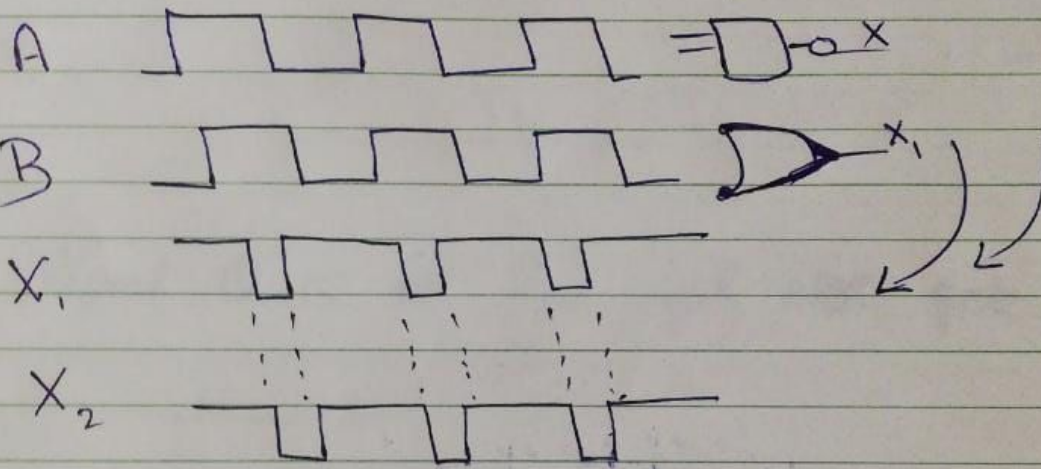
Q15: Determine the output waveform in figure:

Sol



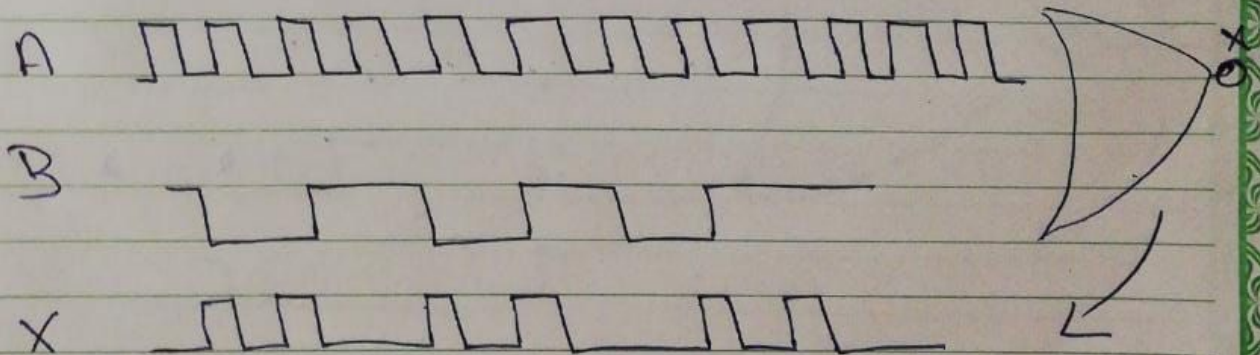
Q16: The two logic symbols shown in figure 11 represent equivalent operations. The difference between the two is strictly from a functional viewpoint. For the NAND symbol, look for two HIGHS on the inputs to give a LOW output. For the negative-OR, look for at least one LOW on the inputs to give a HIGH on the output. Using these two functional viewpoints, shows that each gate will produce the same output for the given set inputs.

Sol



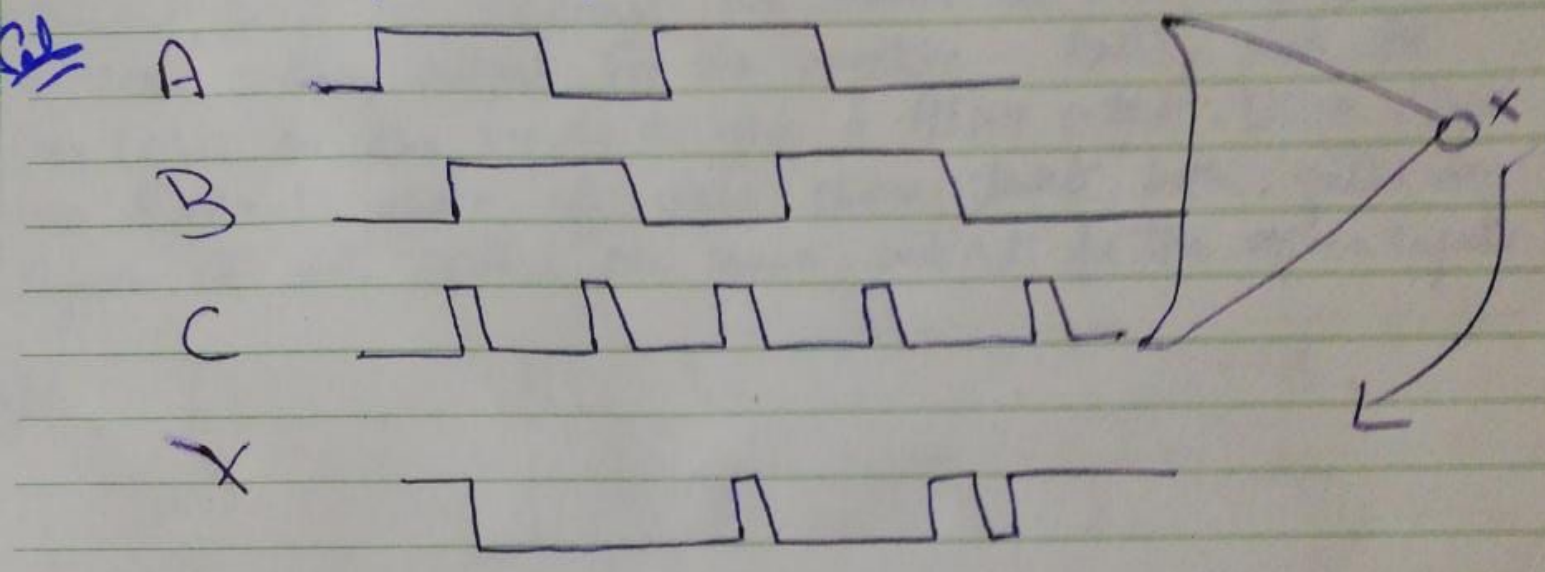
Q17: Repeat Q13 for 2 input nor gate.

Sol

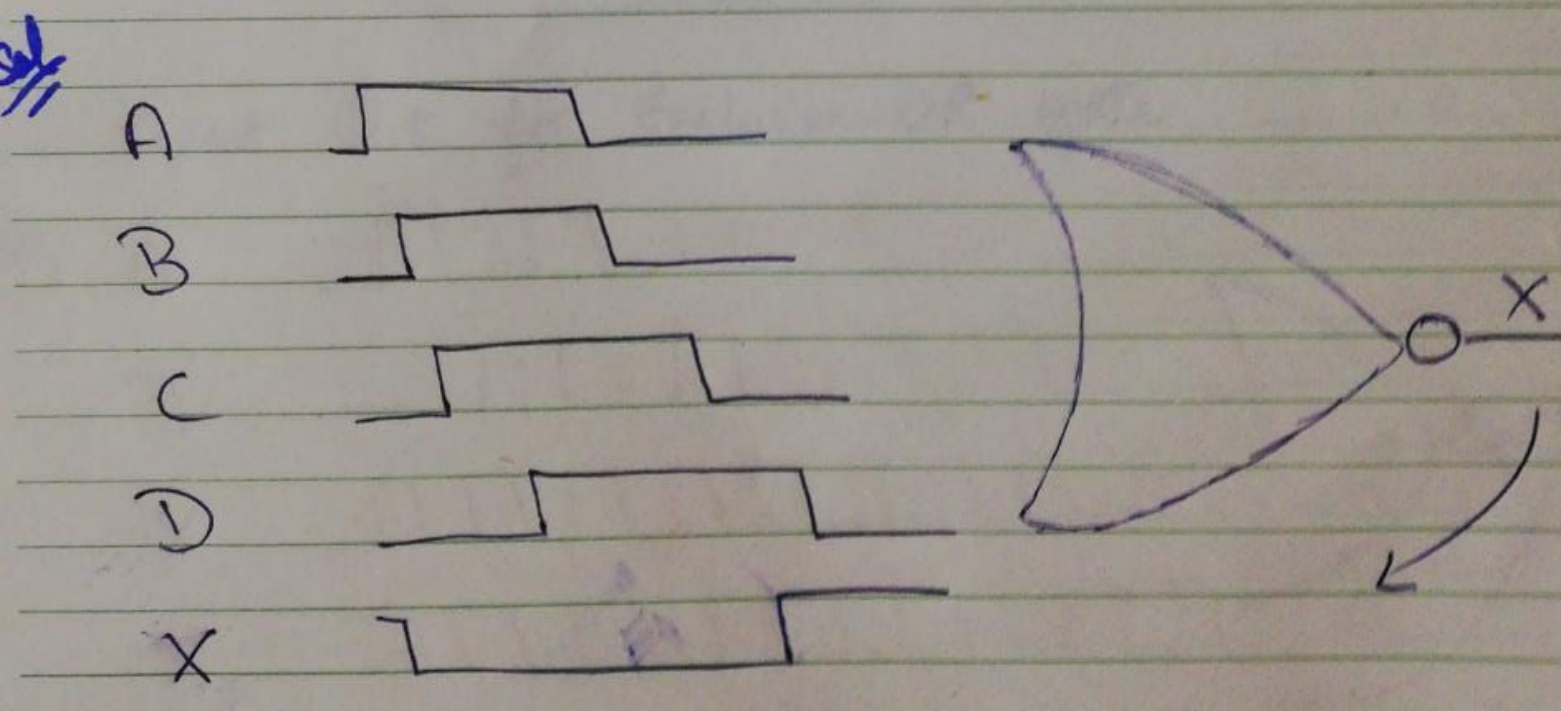


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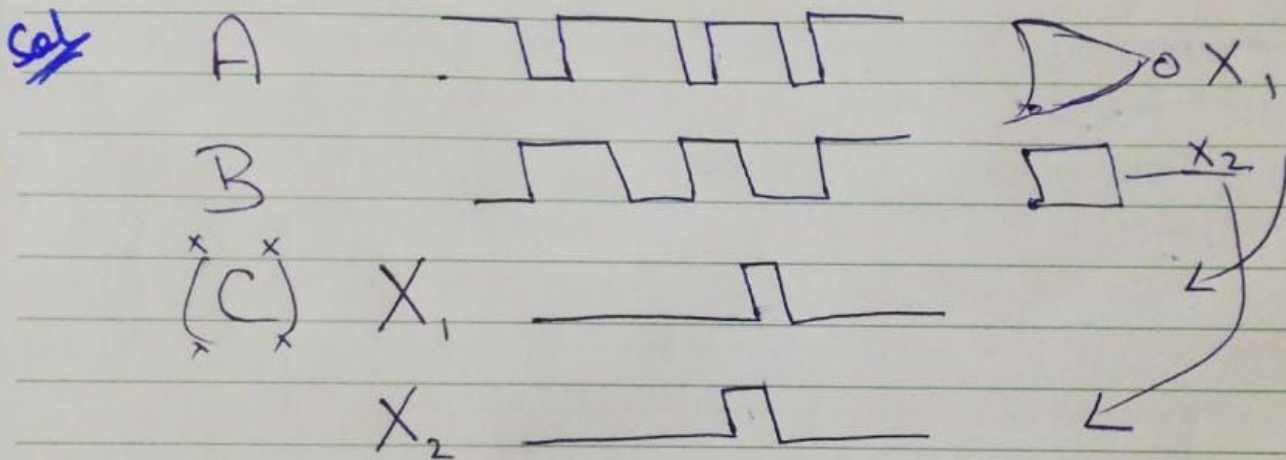
Q18: Determine the output waveform in figure and draw the timing diagram.



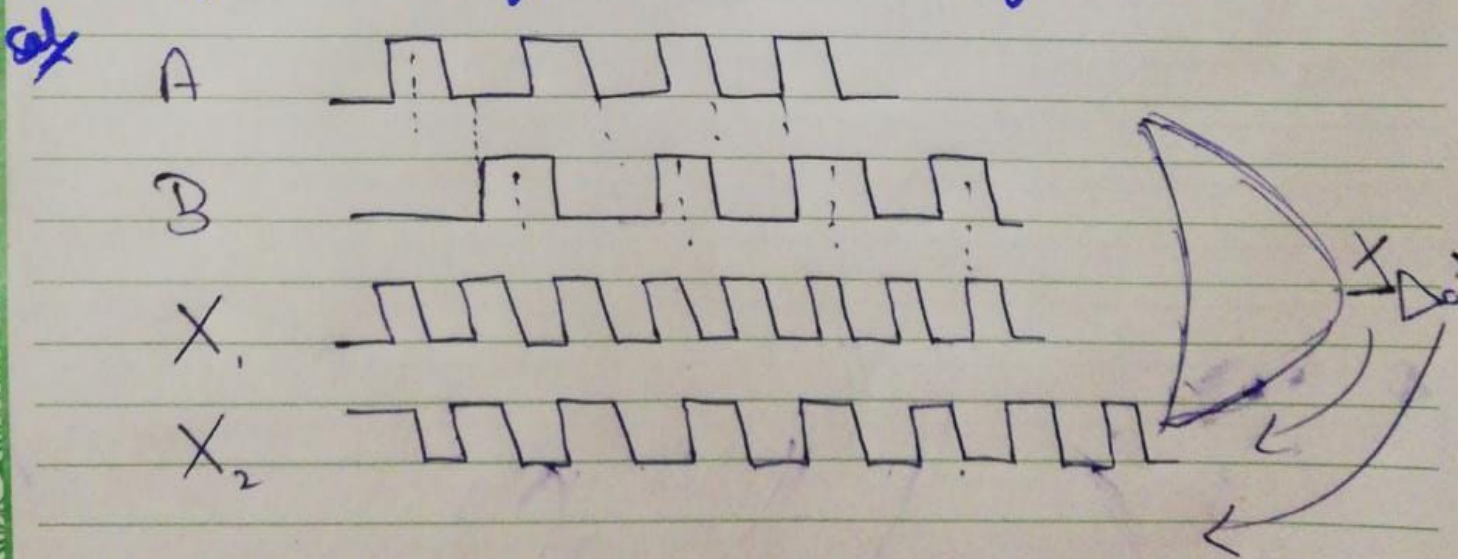
Q19: Repeat Q.15 for four input NOR gate.



Q20: The NOR and the negative-AND symbols represent equivalent operations but they are functionally different. For the NOR symbol, look for at least one HIGH on the inputs to give a LOW on the output. For the negative-AND, look for two LOWs on the inputs to give a HIGH output. Using these two functional points of view, show that both gates in Figure 12 will produce the same output for the given inputs.



Q21: Repeat Q.5 for Exclusive-OR gate



Ques: Repeat Q5 for exclusive NOR gate.

Soln

