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Class : BS SE - B

Subject : DLD

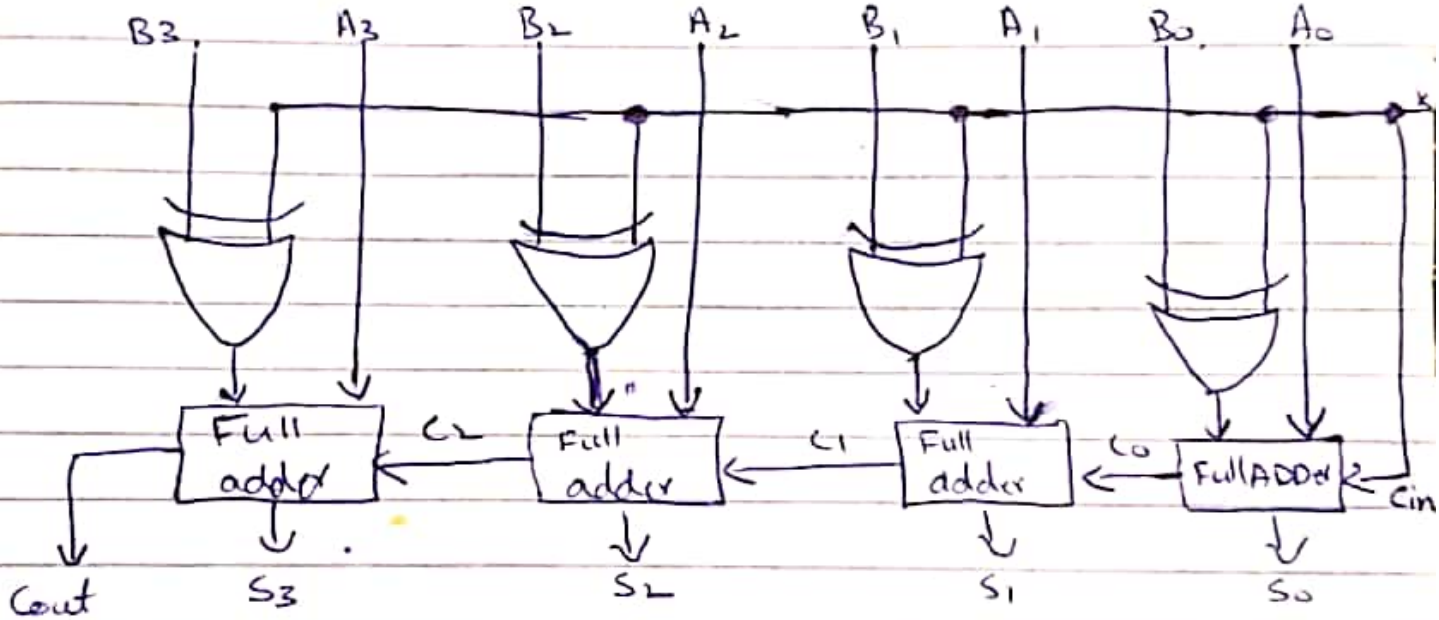
"Final Term

Assciment"

(Q1) Draw and explain the logic diagram

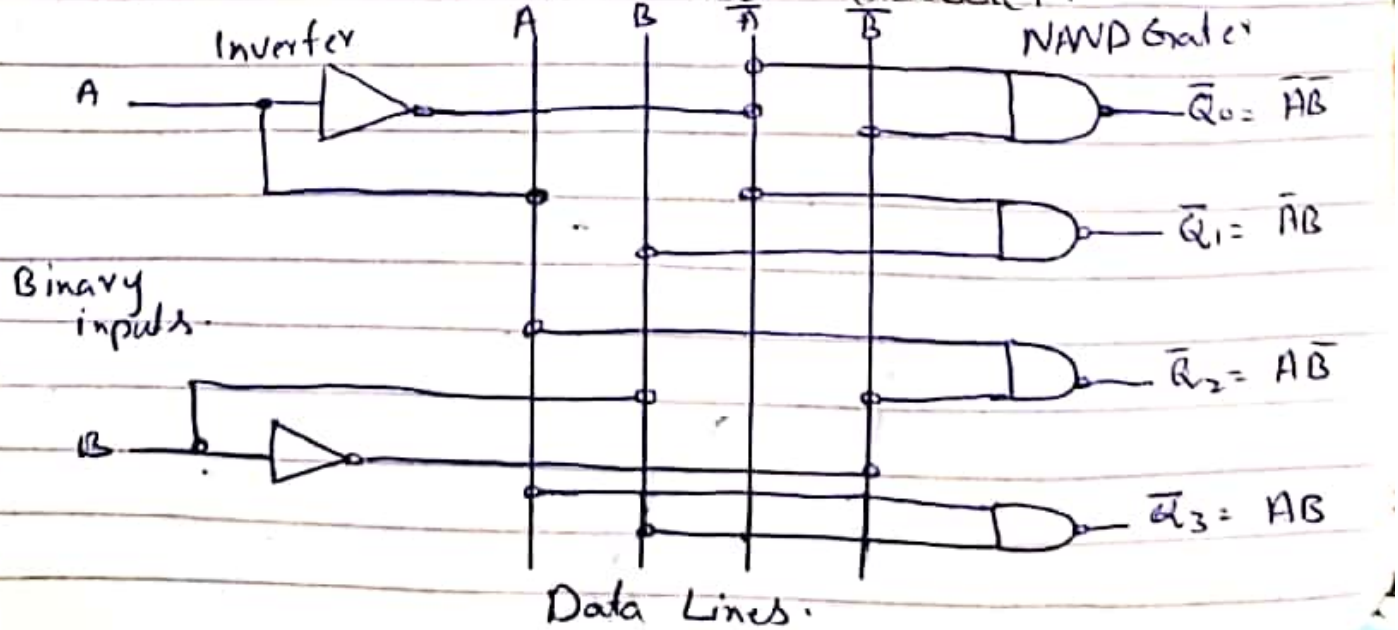
(a) A Circuit for adding or Subtracting two 4-bit numbers.

Ans In Digital Circuit, A binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers in one Circuit itself. it is one of the Components of (ALU)



Q(1)(b)

4 bit active low decoder.



Truth table.

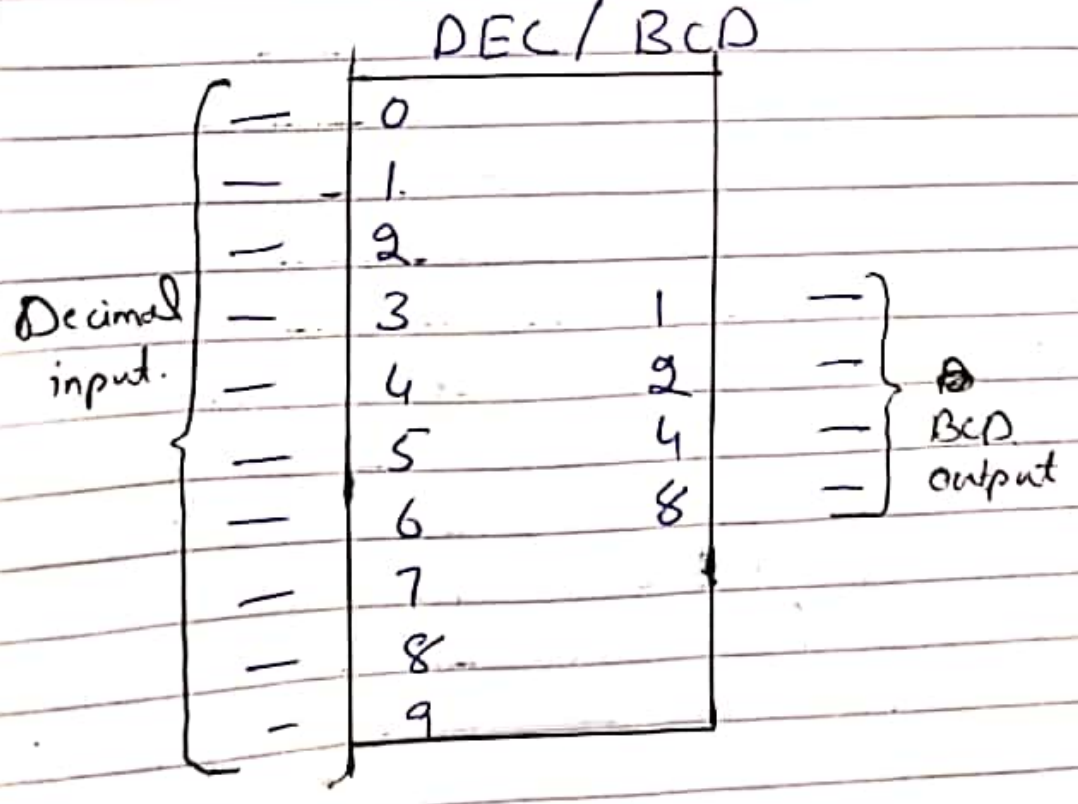
A	B	Q_0	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Q1 (part C)

Decimal to BCD encoder.

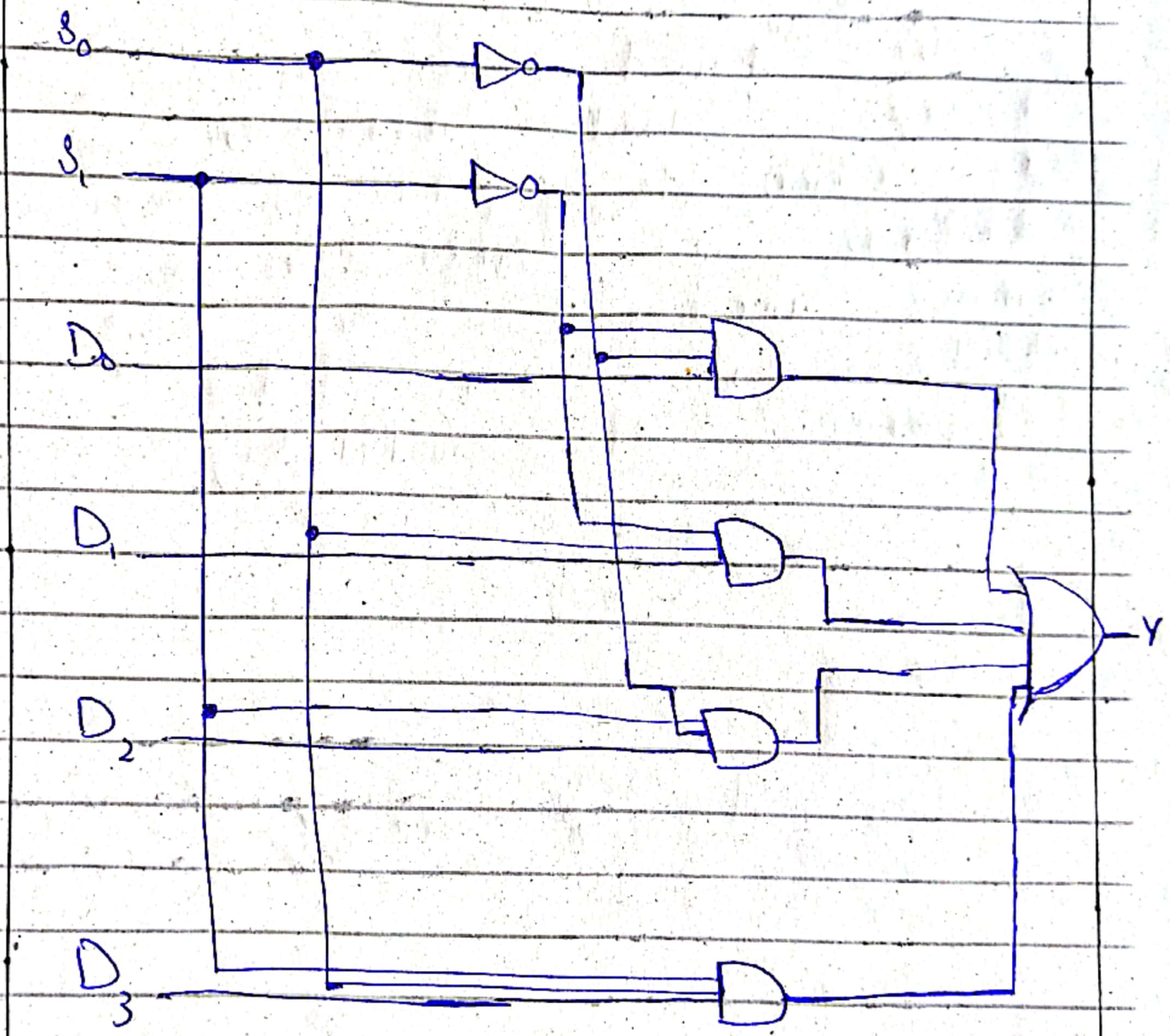
Sol

- encoder has ten inputs - one for each decimal digit and four outputs the outputs indicate the BCD code that represend the active input.

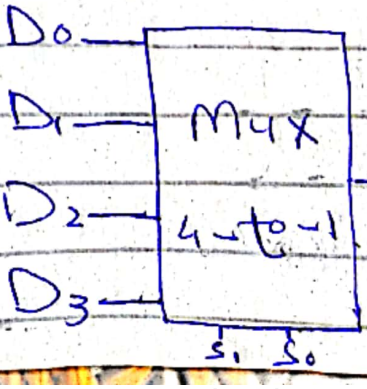


Q2- For 4 input multiplexer ...

A 4 - to - 1 multiplexer is show below:

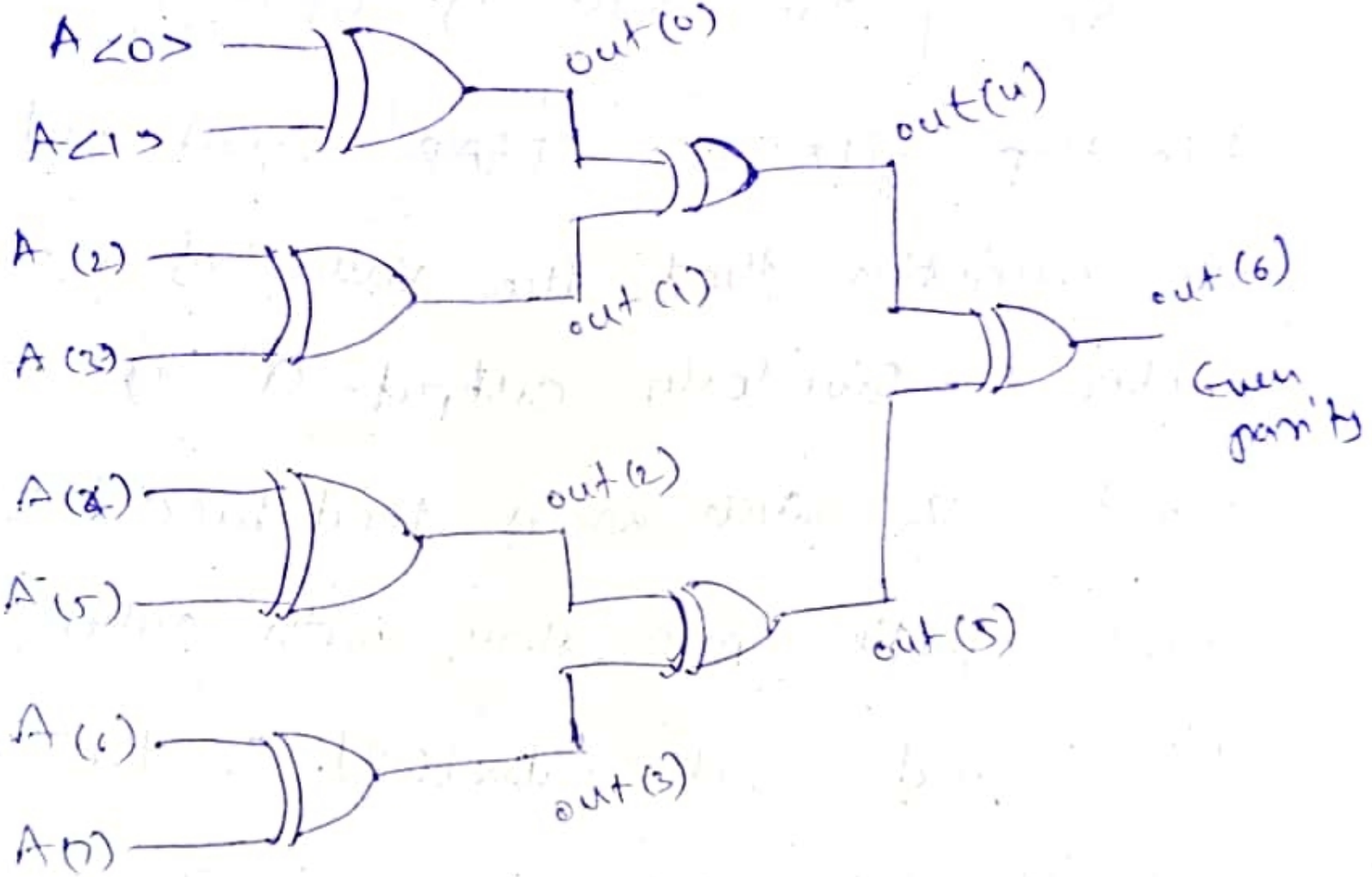


S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



Q3

9- bit parity checker



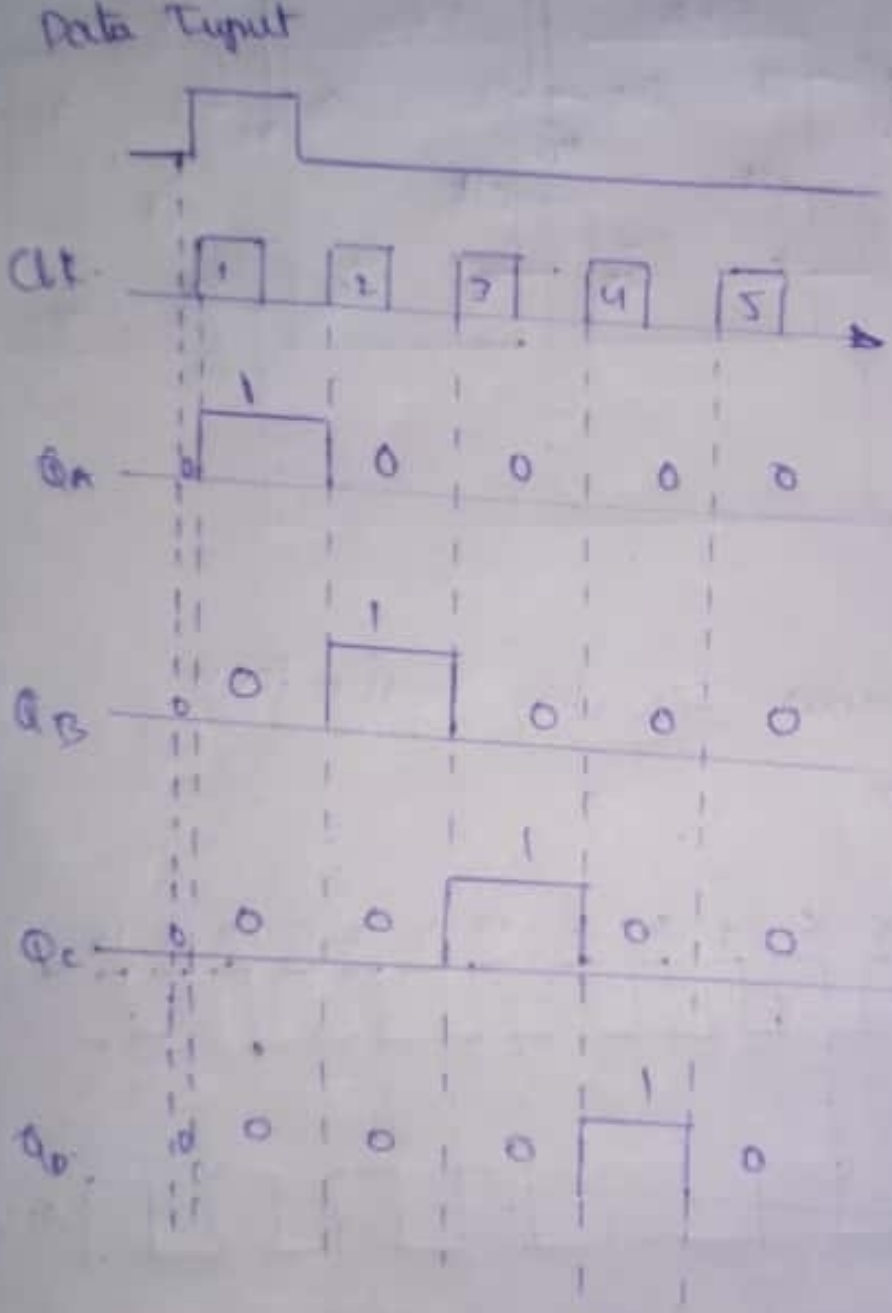
Q4 JK

The behaviour of inputs J and K is same as the S and R inputs of the S-R flip flop.

When both the inputs J and K have a HIGH state, the flip flop switch to the complement state. So for a value of Q=1, it switches to Q=0 and for a value of Q=0, it switches to Q=1.

So, If the value of CP is 1, the flip flop gets a CLEAR signal and with the condition that the value of Q was earlier 1. Similarly output Q' of the flip flop is given as a feed back to the input of the AND along with other inputs like J and clock pulse [CP]. So the output becomes SET. when the value of CP is 1 only if the value of Q' was earlier 1.

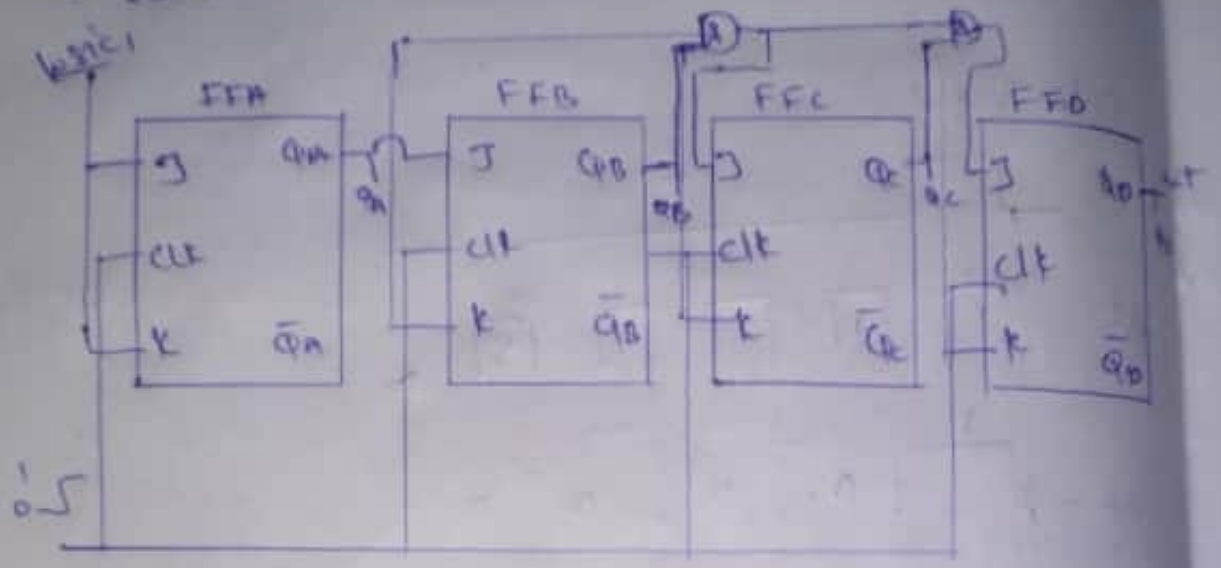
Timing diagram for shift register while Initially cleared.



the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped.

Q6 Logic diagram and timing for 4-bit

Synchronous Counter



4-bit Synchronous Counter wave form

Timing diagram