Date: _____

Name:- M - Daniyal

ID NO:- 17011

Program:- BS (CS)

Subject:- Digital logic design

Instructor:- M- Amin

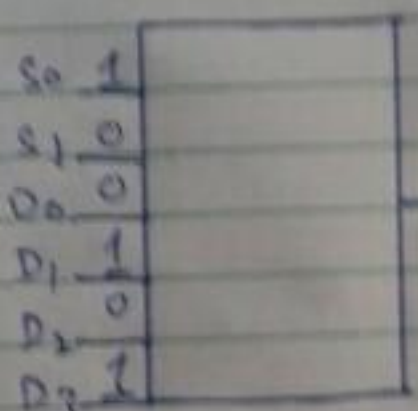
Final- Term Assignment

Date: _____ 1

"Question no2"

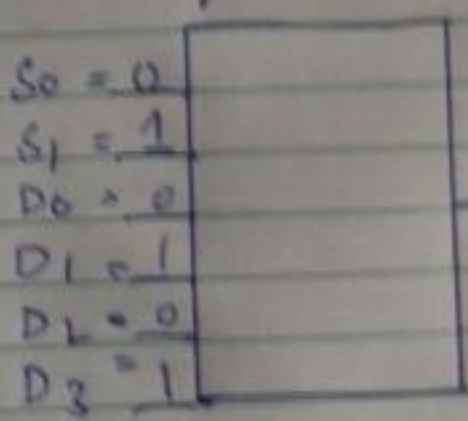
Solution:-

a) $S_0 = 1$, $S_1 = 0$



$S_0 \cdot S_1 = 1_0 \cdot D_0$

b) $S_0 = 0$, $S_1 = 1$



$S_0 \cdot S_1 = D_1$

$0 \cdot 1$

a

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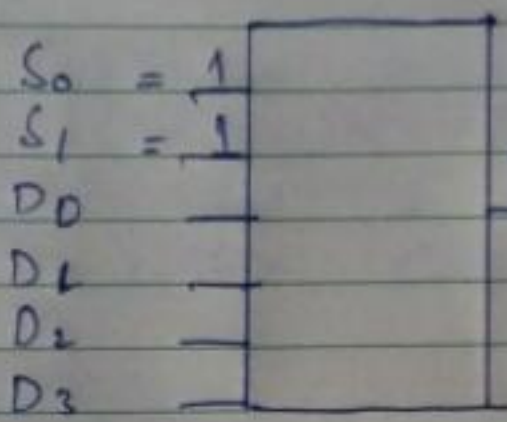
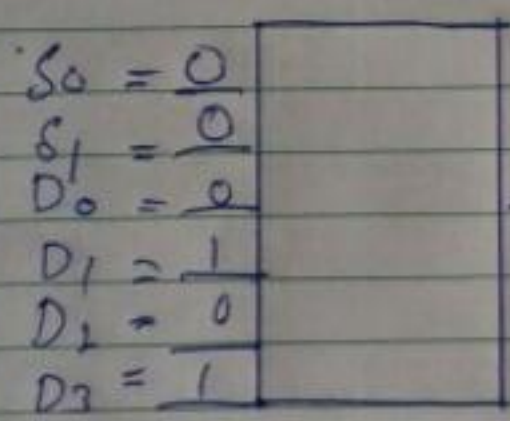
C) $S_0 = 1 \quad S_1 = 1$



$x \; S_0, S_1 = D_2$

1.0

D) $S_0 = 0 \; , \; S_1 = 0$



x

$S_0 . S_1 = D_3$

1.1

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"Question no 3"

Timing diagram in figure 01 shows input to a 4-bit parity cheackar. Draw the Σ even and Σ odd output for the even parity Cheackar.

Solution:-

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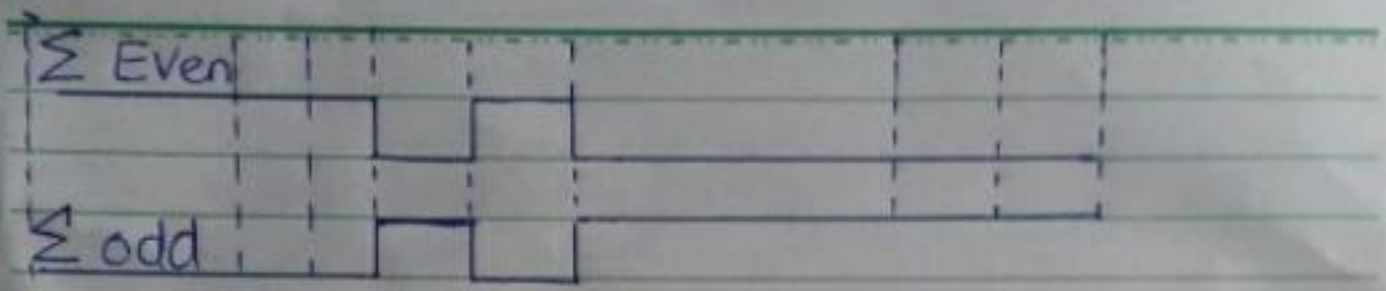

output.

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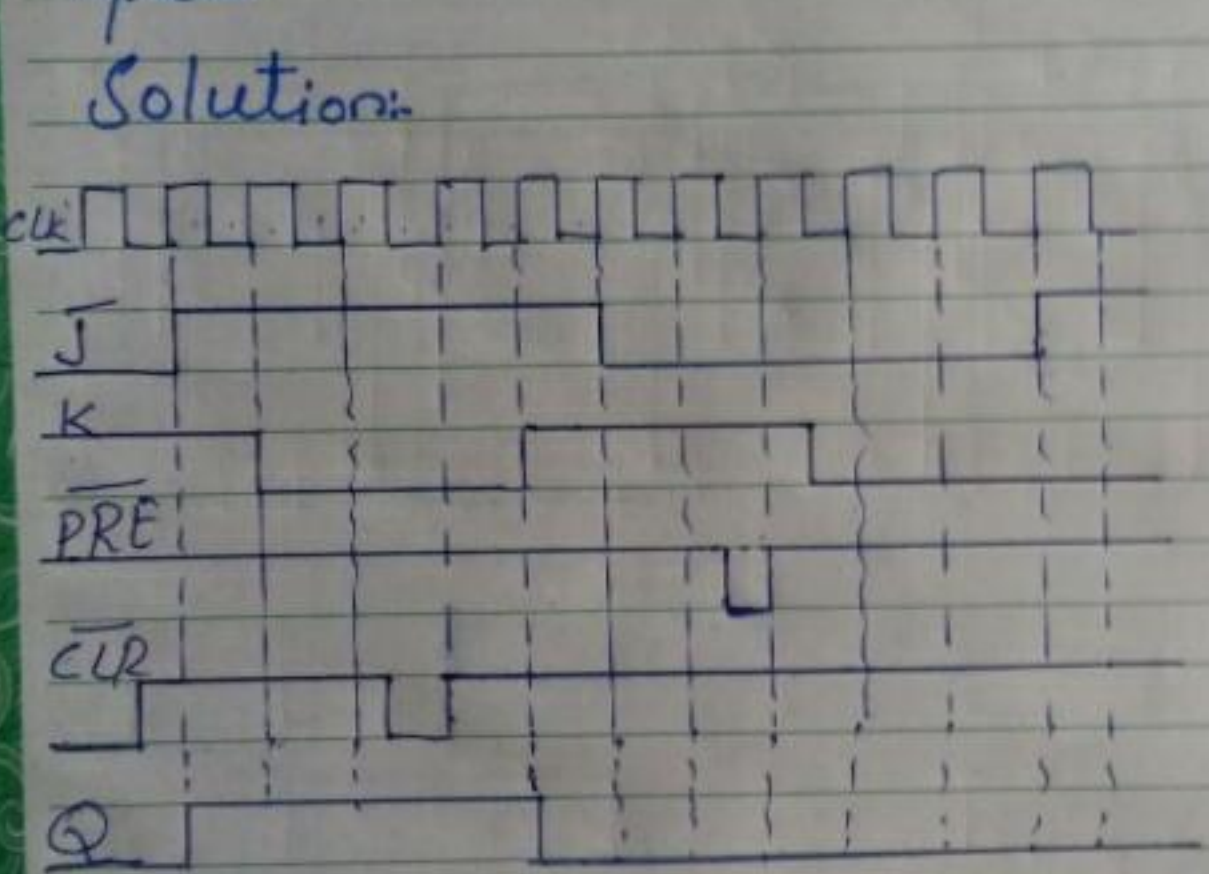
"Question no 4"

The wave form in figure 032 to draw the timing diagram for J, K, CLK, PRE, CLR inputs.

Solution:-



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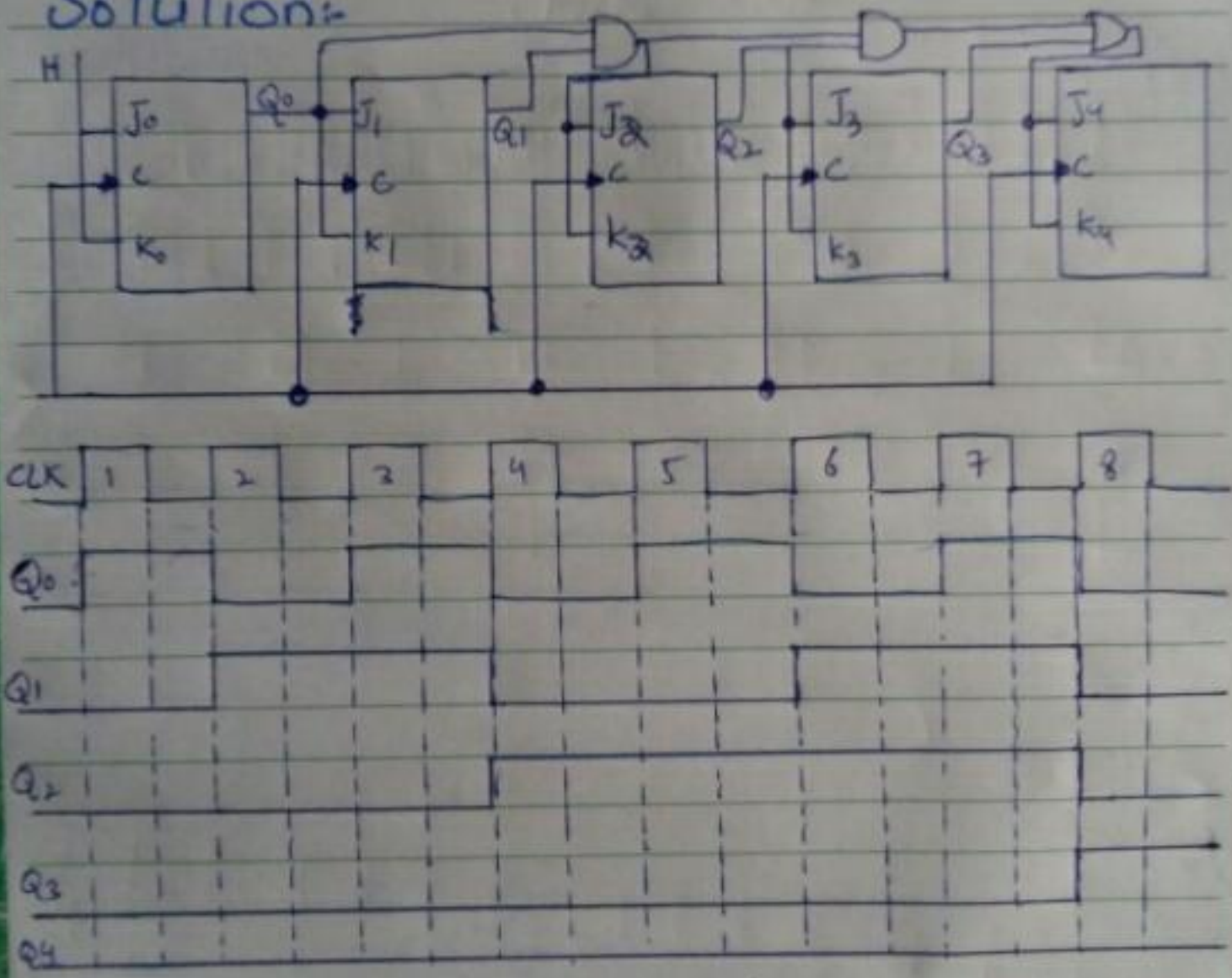
"Question no 5"

Use the waveforms in Fig 03 to draw the timing diagram for the parallel outputs

Solution:-



Date: _____

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"Question no 6"

Draw the logic diagram and timing diagram for the 4-Stage Synchronous binary Counter.

Solution: