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Paper Computer Architecture.

QUESTION#1.

* Give answers to each of the following.

Discuss the concept of word, addressable units, and unit of transfer for internal memories.

Ans) Word:-

The natural unit of organization of memory. The size of word is usually equal to the no. of bits used to represent an integer and to the instruction length.

ADDRESABLE UNITS :-

In some systems, the addresable unit is the word. However, many systems allow addressing at the byte level. In any case, $2^A = N$.

UNIT OF TRANSFER :-

for main memory, this is the number of bits readout of or written into memory at a time. The unit of tranfer need not equal a word or an

(b) How the least recently used (LRU) and least frequently used (LFU) replacement algorithms are implemented for a cache memory with two-way set associative mapping?

Ans) Probably the most effective is least recently used (LRU): Replace that block in the set that has been in the cache longest with no reference to it. for two way set associative, this is easily implemented. Each line includes a USE Bit. B when a line referenced, its use bit is set to 1 & and the use bit in other line is set to 0. When a block is to be read into the set, the line whose use bit is 0 is used. Because we are assuming that more recently used memory locations are more recently used likely to be referenced, LRU should give the best hit ratio. LRU also is relatively easy to implement for a fully associative cache. The cache mechanism maintains a separate list of indexes to all the line in the

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cache. When the line is referenced, it moves to the front of the list. For replacement, the line at the back of the list is used. Because of its simplicity of implementation, LRU is the most popular replacement algorithm. Still another possibility is least frequently used (LFU) Replace that block in the set that has experienced the fewest references. LFU could be implemented by associating a counter with each line. A technique not based on usage is to pick a line at random from among the candidate lines. Stimulation studies have shown that randomly replacement provides only slightly inferior performance to an algorithm based on usage [SMIT82]

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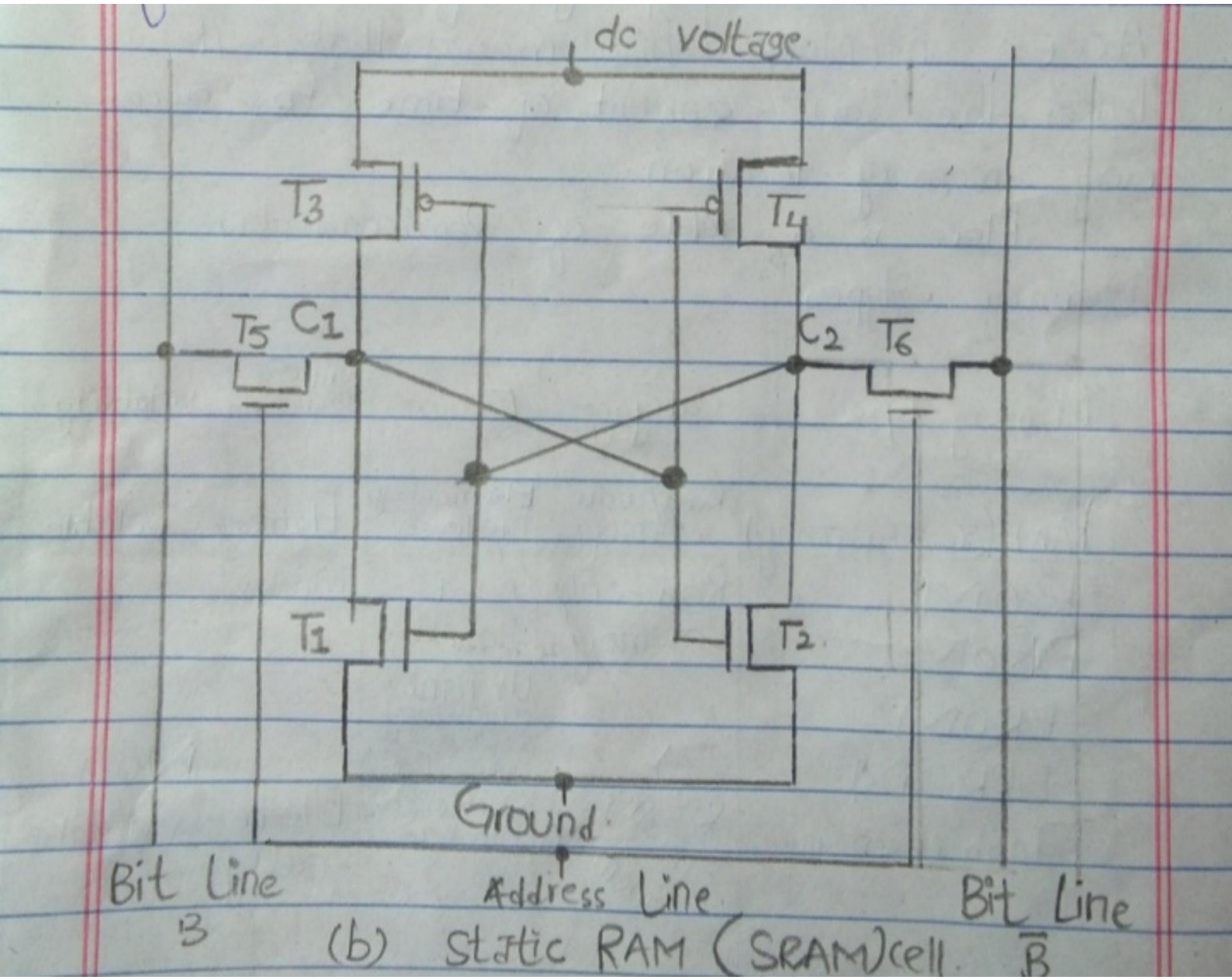
(c) How read and write operations are performed in SRAM cell?

* READ OPERATION:-

In SRAM, for any operation to be performed, the word line should be high. To perform read operation initially.

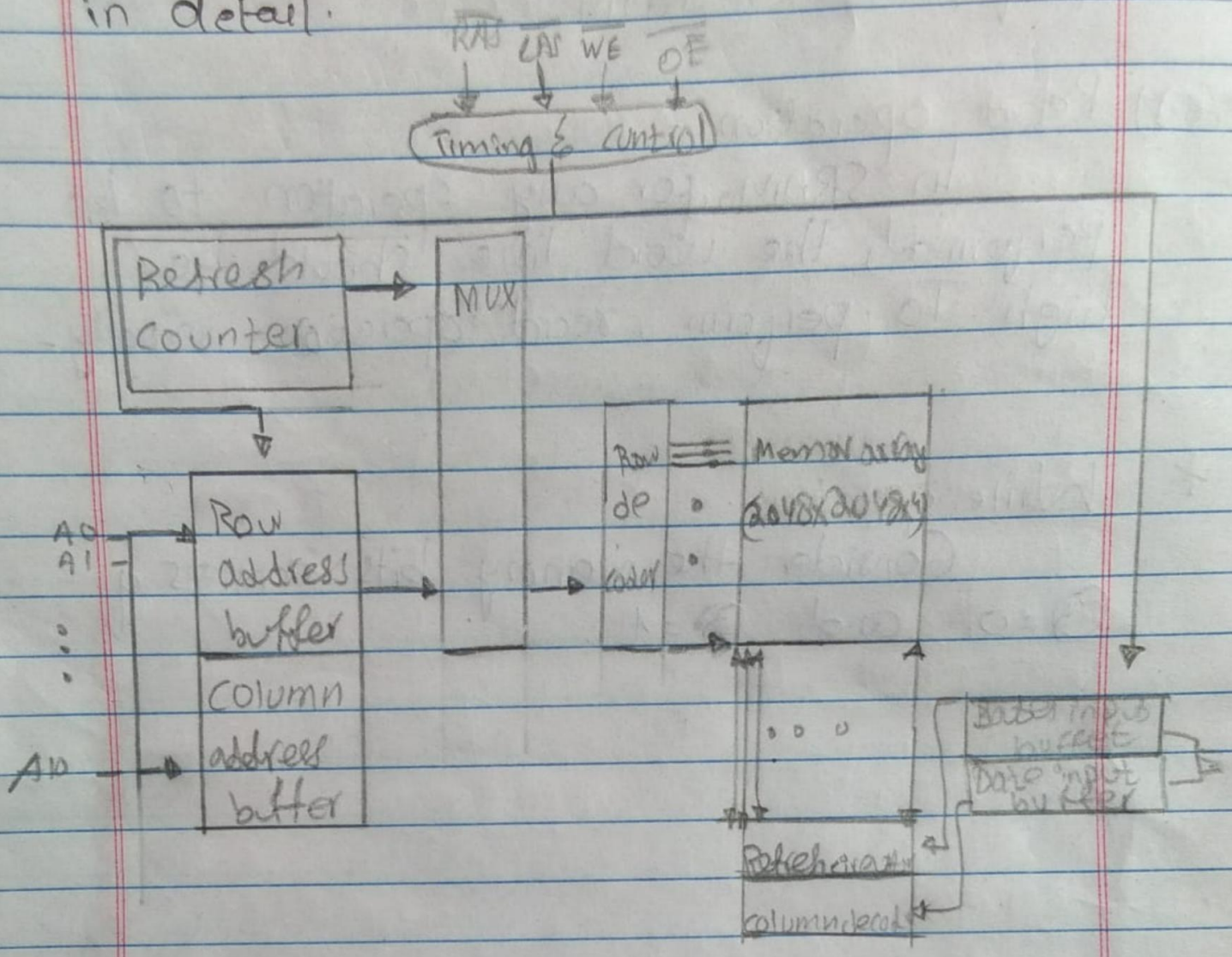
* Write Operation:

Consider the memory bits consists of Q=0 and Q=1.



(b) Static RAM (SRAM) cell

d) Discuss 16-Mbit DRAM (4M×4) organization in detail.



Because only 4 bits are read/written to this DRAM, there must be multiple ~~to~~ DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for ~~resistivity~~ refreshing is in effect to disable the DRAM chip while all data cells are refreshed.

The refresh counter step through all of the row values. This causes each cell in row to be refreshed.

(e) What are the reasons for DVDs greater capacity over CD?

Ans) The DVD's greater capacity is due to three differences from CDs.

(1)

Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 um and the minimum distance blw pits along the spiral is 0.834 um. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 um & minimum distance between pits of 0.4um. The result of these two improvements is about a seven fold increase in capacity to about 4.7 GB.

(2)

The DVD employees a second layer of pits and lands on top

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of the first layer. A dual-layer DVD has a semi-~~conducter~~ reflective layer on top of the reflective layer, and by adjusting focus the lasers in DVD drives can read each layer separately.

The technique almost doubles the capacity of the disk, to about 8.5 GB. The lower reflectively of the second layer limits its storage capacity so that a full doubling is not achieved.

(3)

The DVD-ROM can be two sided, where as data are recorded on only one side of a CD. This brings total capacity upto 17 GB.

Q#2 Difference each of the following in detail.

a) EEPROM and flash memory.

EEPROM	flash memory
* EEPROM stands for electrically erasable programable read only memory.	Flash memory is a non volatile memory chip used for a storage and for transfering data.
* EEPROM device can erase only byte of memory at any time.	Flash memory can only erase an entire chunk, or "sector" of memory at a time.
* EEPROM user Nor type memory.	Flash memory uses NAND type memory.
* EEPROM is byte wise erasable	Flash is block wise erasable.

b) Hard failure and Soft error in Semiconductor memories.

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear

Where as:-

Soft error is a random, non-destructive even that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

C Read and write mechanism for magnetic disk.

READ:-

The traditional read mechanism exploits the fact that a magnetic field moving relate to a coil produces an electrical current in the coil. When the surface of the disc passes under the head, it generates a current of the same polarity as the one already recorded. Such single heads are used in floppy discs systems and in older rigid disk systems. The read head consists of a partially shielded magnet erosistive (MR) sensor. The MR design allows higher frequency operation which equation to greater storage densities and operating speeds.

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WRITE:-

The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field. Electric pulses are sent to the write head, & the resulting magnetic patterns are recorded on the surfaces below, with different patterns for positive and negative currents. An electric current in the wire induces a magnetic field across the gap, which in turn magnetizes a small area of the recording medium, reversing the direction of the magnetization on the recording medium.

d) Parallel access and independent access RAID Schemes.

→ PARALLEL ACCESS:-

In parallel access array, all member disks participate in the execution of every I/O request. Typically the spindles of the individual drives are synchronised so that each disk head is the same position on each disk at any given time.

As in the other RAID Scheme, data stripping is used, in the case of RAID 2 & 3 the strips are very small, often as small as a a single byte or word.

Independent Access RAID:

In an independent access array, each member disk operates independently so that separate I/O requests can be satisfied in parallel Because of this, independent access array are more suitable

for applications that require high I/O requests routes and are relatively less suited for application that require high data transferates.

* As in the other RAID schemes data stripping is used in case of RAID 4 through 6, strips are relatively large.

(e) HD DVD AND BLU-RAY DVD:-

Ans) HD DVD players have been much chapter than Blu-ray machines, but Blu-ray disc have more storage space and more advanced protection against piracy.

* Both versions deliver sharp resolution
* Blu-ray has 25 GB capacity (50 GB for dual-layer) and is more expensive.
* HD-DVD has 15 GB (30 GB for dual layer) and is cheaper than Blue-RAy.

QUESTION # 3

Write note on each of the following.

a) MEMORY ACCESS METHODS:-

There are four types of memory access methods

1. Sequential Access:-

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single linked list. The access time depends on the location of the data.
Applications of this sequential memory access are magnetic tapes, magnetic disk and optical memories.

2. Random access:-

In this method, any location of the memory can be accessed randomly like accessing in Array. Physical locations are independent in this access method.
Applications of this random memory access are RAM & ROM

3. Direct Access:-

In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. The access time depends on both the memory organization and charac-teristics of storage technology. The access is semi-random or direct.

Application of this direct memory access is Magnetic hard disk, read/write header.

4. Associate Access:-

In this memory, a word is accessed rather than its address. This access method is a special type of random access method.

Application of this direct memory access is Cache memory.

(B) PRINCIPLE OF LOCALITY:-

The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

"OR"

An implication of locality is that we can predict with reasonable accuracy what instructions and data a program will use in the near future based on its accesses in the recent past

(C) POSSIBLE APPROACHES TO CATCH COHERENCY:

possible approaches to catch coherency include the following.

- Bus watching with write-through: Each cache controller monitor the address lines to detect write operation to memory by other bus masters. if another master writes to a location in shared memory that also resides in the cache memory, the catch controller invalidates the cache entry. This strategy depends on the use of a write-through policy by all cache controllers.

- Hardware transparency:- Additional hardware is used to ensure that all updates to main memory

Cache are reflected in all caches. Thus, if one processor modifies a word in its cache, this update is written to main memory, in addition any matching words in other caches are similarly updated.

- Non-cachable memory:- only a portion of main memory is shared by more than one processor, and this is designated as non-cacheable. In such a system, all accesses to shared memory is never copied into the cache. The non-cacheable memory can be identified using chip select logic or high address bits.

(D) PRACTICAL ISSUES PECULIAR TO SSDs.

There are two peculiar issues to SSDs that are not faced by HDDs.

* SDD performance has a tendency to slow down as a device is used:-
* The entire block must be read from the flash memory and placed in a RAM buffer.

* Before the block can be written back of flash memory, the entire block of flash memory must be erased.
* The entire block from the buffer is now written back to the flash memory.

* flash memory becomes unusable after a certain number of write.

* Techniques for prolonging life.
* front-ending the flash with a cache to delay and group write operations.
* using wear-levelling algorithms that evenly distribute writes across block of cells.
* Bad block management techniques.
* Most flash devices estimate their own remaining life times so system can anticipate failure and take preemptive action.

(e) CD read and write operation:

READ:-

information is retrieved from a CD or CD-ROM by a low

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powered laser housed in an optical disk player, or device unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit. Specifically if the laser beam falls on a pit, which has a somewhat rough surface, the light scatters and a low intensity is reflected back to the source. The areas between pits are called lands.

A land is a smooth surface, which reflects back at higher intensity. The change blw pits and lands is detected by a photo sensor and converted into a digital signal. The sensor tests the surface at regular intervals. The beginning or end of a pit represents a 1; When no change in elevation occurs blw intervals, a 0 is recorded.

Write:

Recall that on a magnetic disk, information is recorded in

Concentric tracks.

With the simplest constant angular velocity (CAV) system, the number of bits per track is constant. An increase in density is achieved with multiple zoned recording, in which the surface is divided into a no. of zones, with zones farther from the centre containing more bits than zones closer to the center. Although this technique increases capacity. It is still not optimal.

QUESTION #4

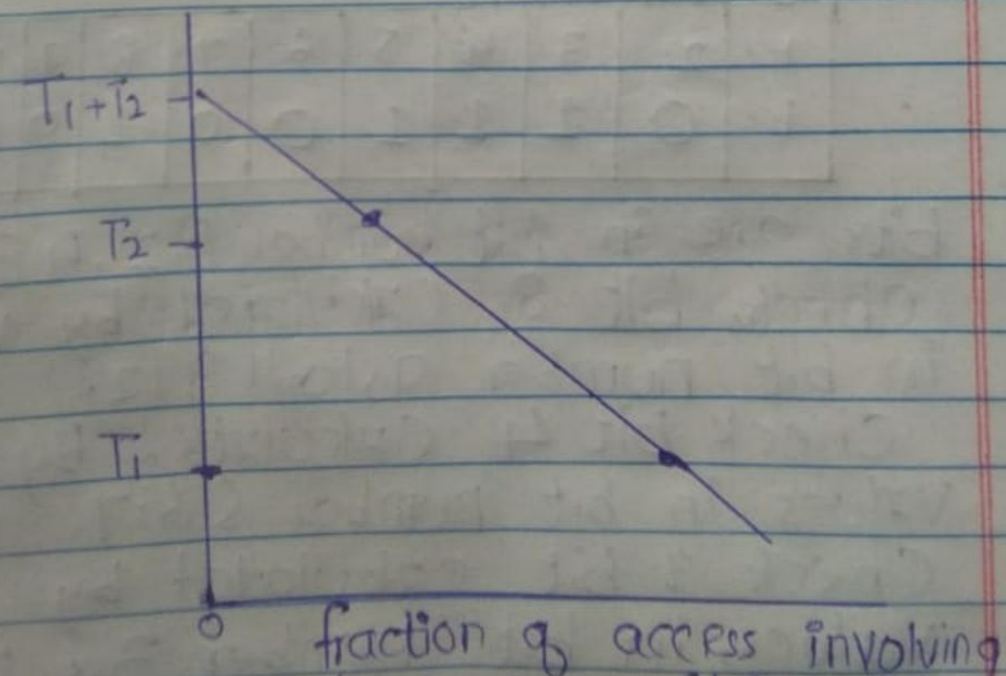
Solve the following numericals.

(a) In our example we suppose 95% of the memory accesses are found in level 1. Then the average time to access a word can be expressed as

$$(0.95)(0.01\,\mu s) + (0.05)(0.01\,\mu s + 0.01\,\mu s) =$$

$$0.0005 + 0.0055 = 0.015\,\mu s.$$

The average access time is much closer to 0.01 μs then to 0.1 μs as desired.



(b) ANSWER

Main memory address = 9F3A7Ch.
in binary.
1001111100111010111011100

Tag	Set	word
100111110	011101011101	00

← 9bits → ← 13bits → 2bits.

(C) ANSWER

M = 8
$2^K \geq (K + M)$
$2^4 \geq (4 + 8)$
$16 \geq 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

bits are in bit number 1, 2, 4 & 8
Check bit 8 calculated by values in bit number 9, 10, 11 & 12.
Check bit 4 calculated by values in bit number 5, 6, 7 & 12.
Check 1 bit calculated by values, in bit number 3, 5, 7, 9, 10, & 11

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Thus the check bits are 1011.

(d) ANSWER.

7200 revolution in 60sec.
1 revolution in 60/7200
= 6Ms.

1 revolution = covering one entire track = 500 sector.

500 Sector = 6ms.
1 sector = 8Ms

Now there are 2 different things.

2500 Sectors so time 2500 x 8ms
= 20Ms.
1.28Ms = 1342177.28 bytes.
2622 = 20.9ms

Case ① 4+2+20 = 26Ms.
Case ② 4+2+20+ 976 26.976Ms