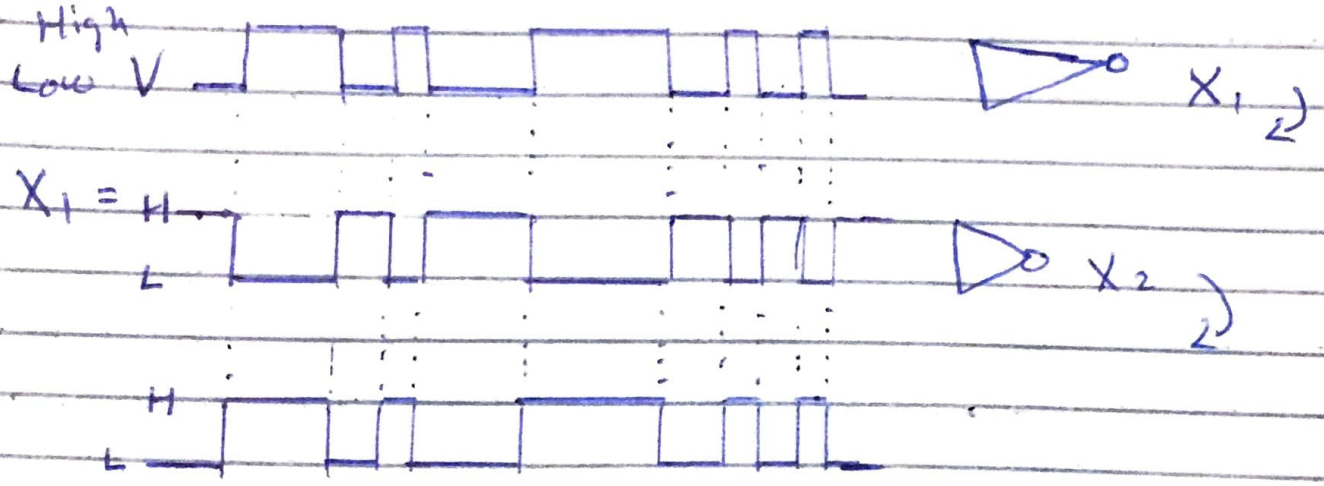
Digital Logic Design

Assignment 2
Sir. Muhammad Amin

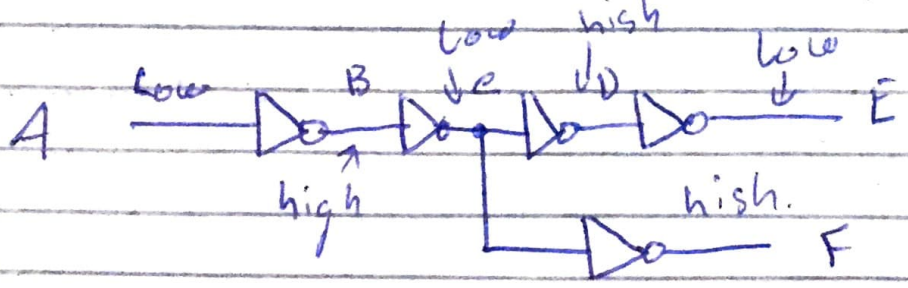
HASSAN MEHDI
15453
Csc-201

Q1: The input waveform in figure is applied to a system of two inverters connected in series. Draw the output waveform across each inverter in proper relation to the input.

Sol



Q2: A combination of inverters is shown in figure if a low is applied to the point A, determine the ~~waveform~~ output at point E and F

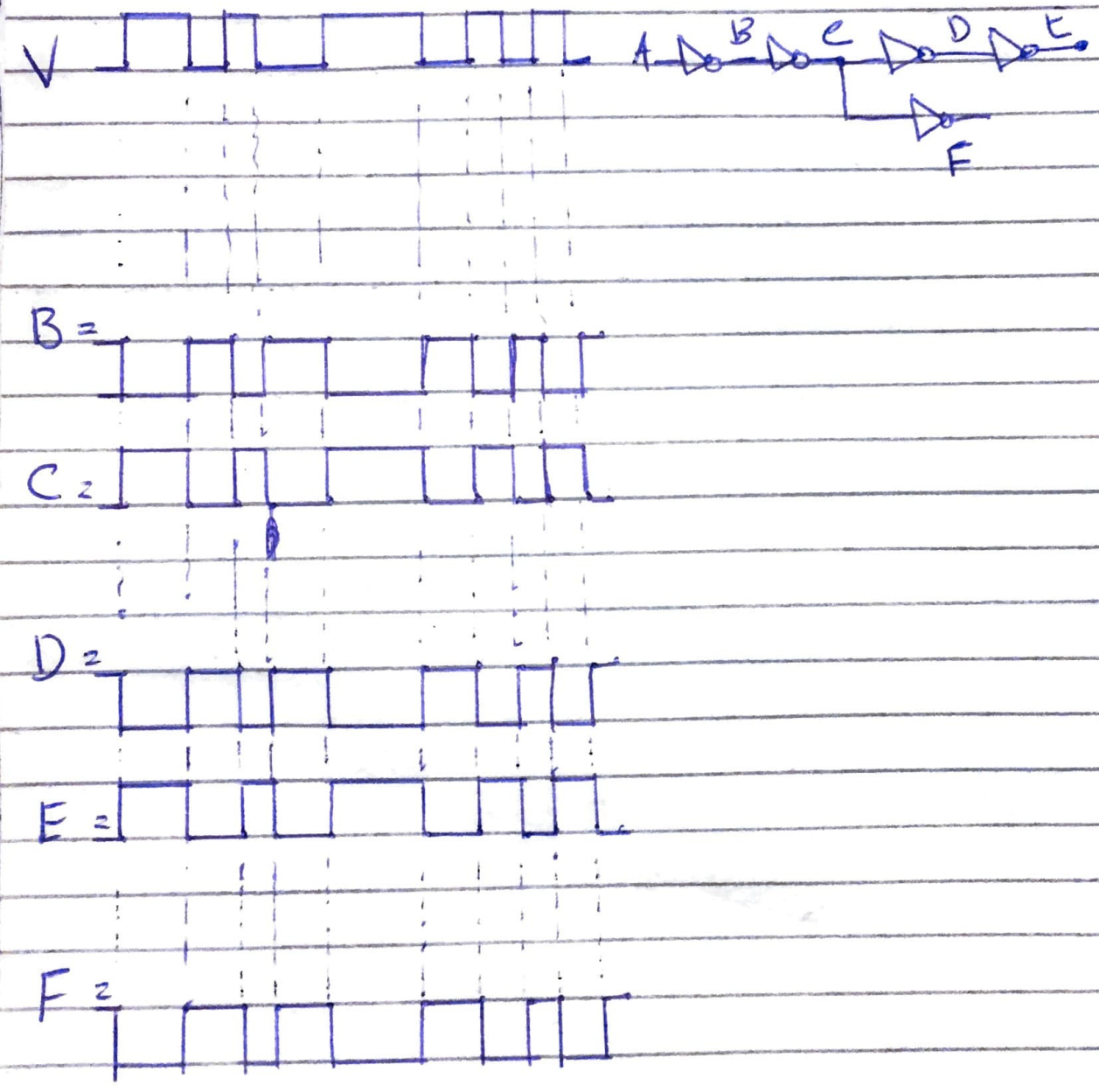


E = low

F = High

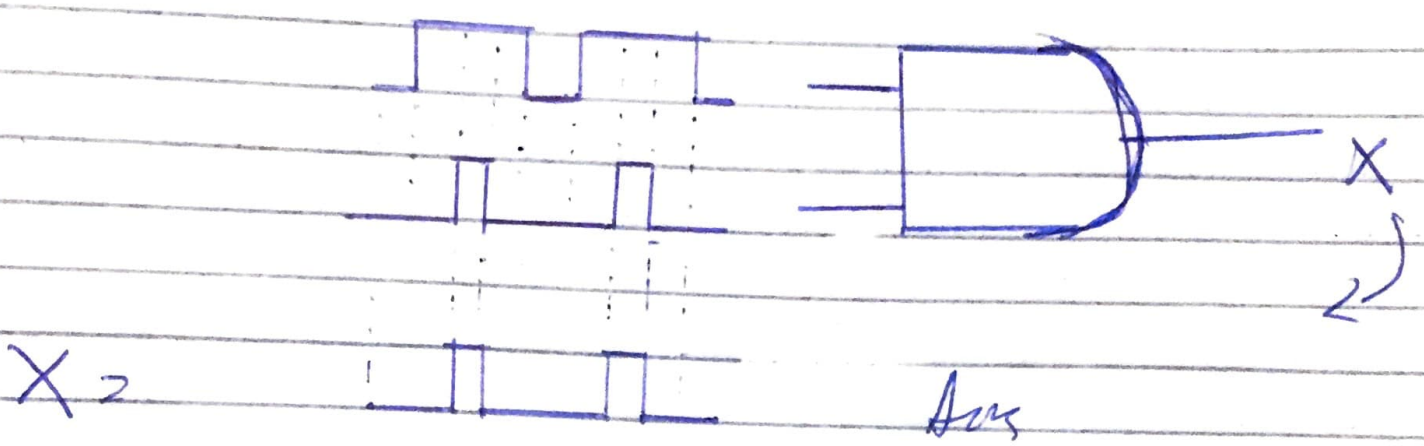
Q3: if waveform in Q_1 is applied to figure in Q_2 at point A. Determine the waveform from Point B to F.

Sol)



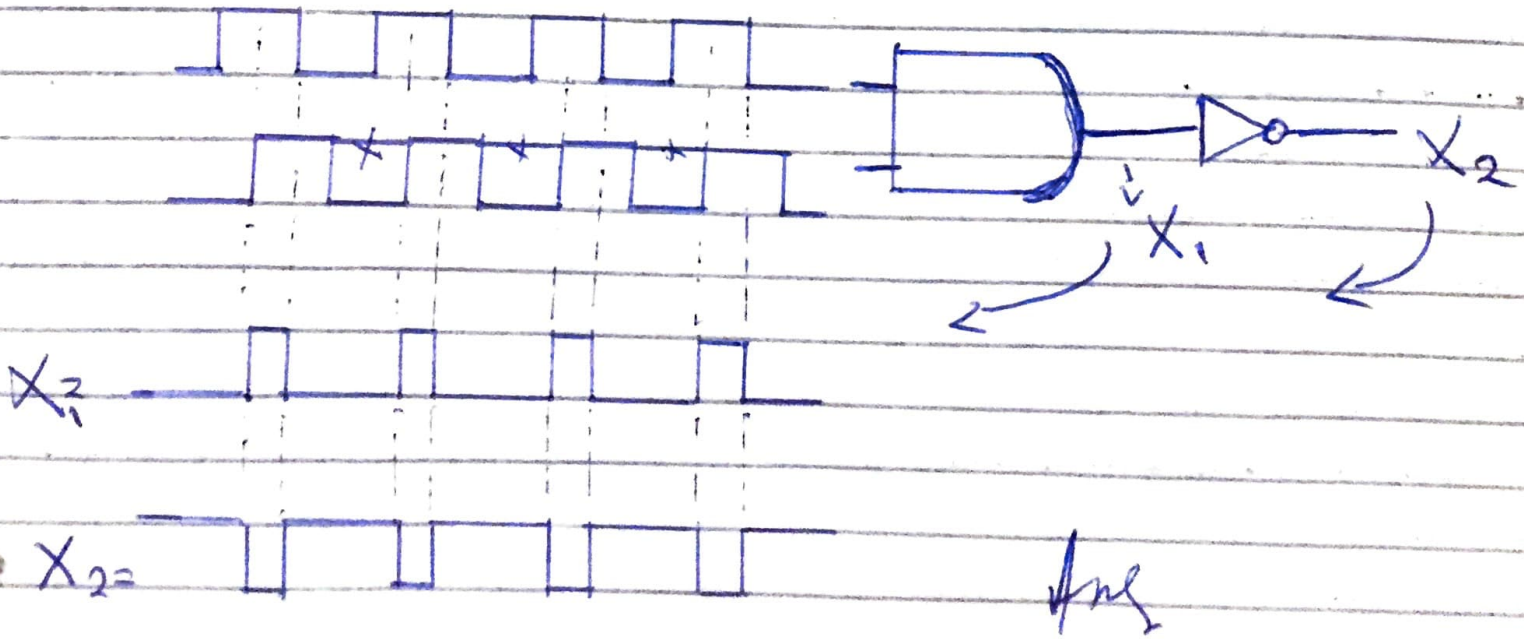
Q4: Determine the output, X for a 2 input AND gate with the input waveform in figure.

Ans



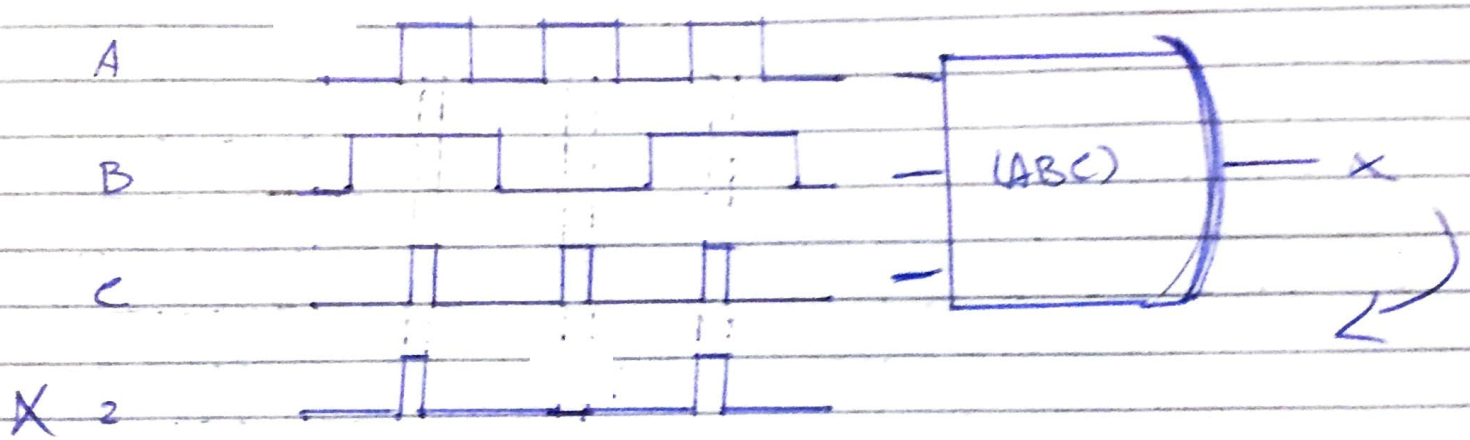
Ans

Q5: The waveform in figure are applied to point A and B of a 2 input AND gate followed by an inverter. Draw the output waveform.

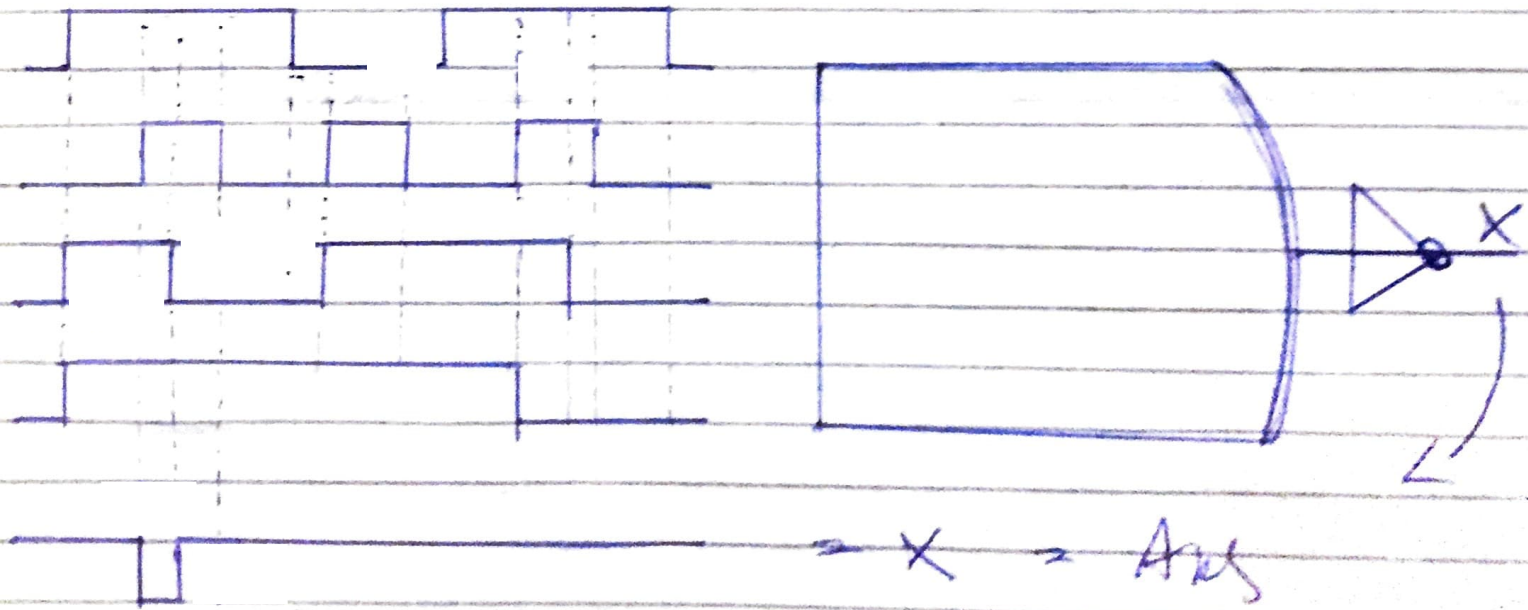


Ans

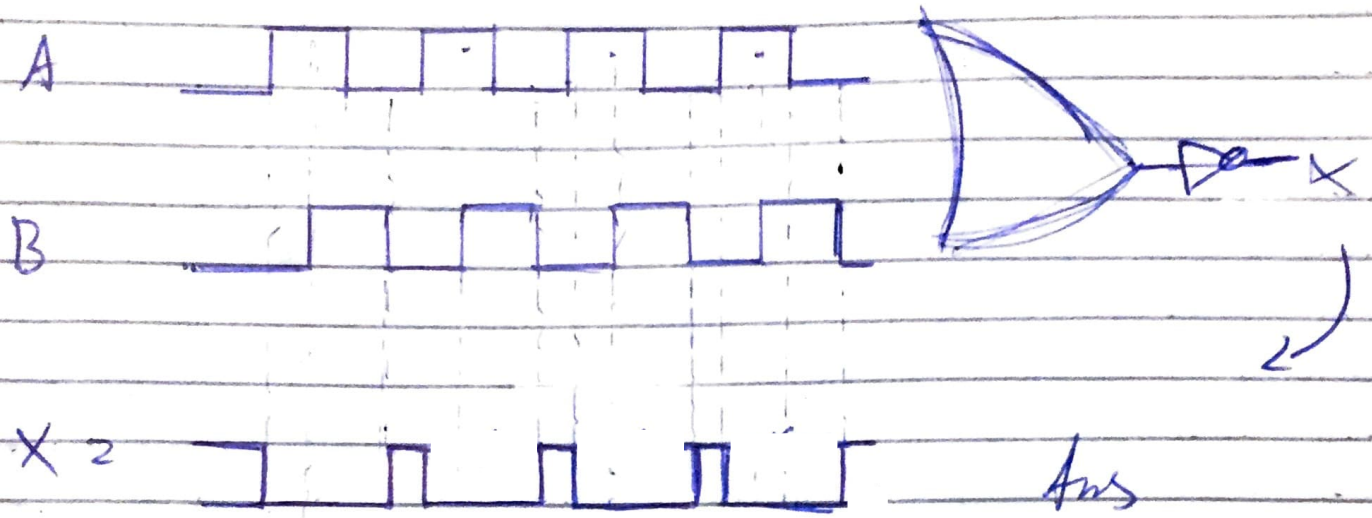
(6) The input waveform applied to 3-input ~~NAND~~ AND gate are as indicated in figure. Show the output waveform in proper relation to the inputs with the time diagram.



Q7: The input waveform applied to a 4 input AND ~~gate~~ gate as indicated in figure, the output is fed to an inverter Draw the net output.

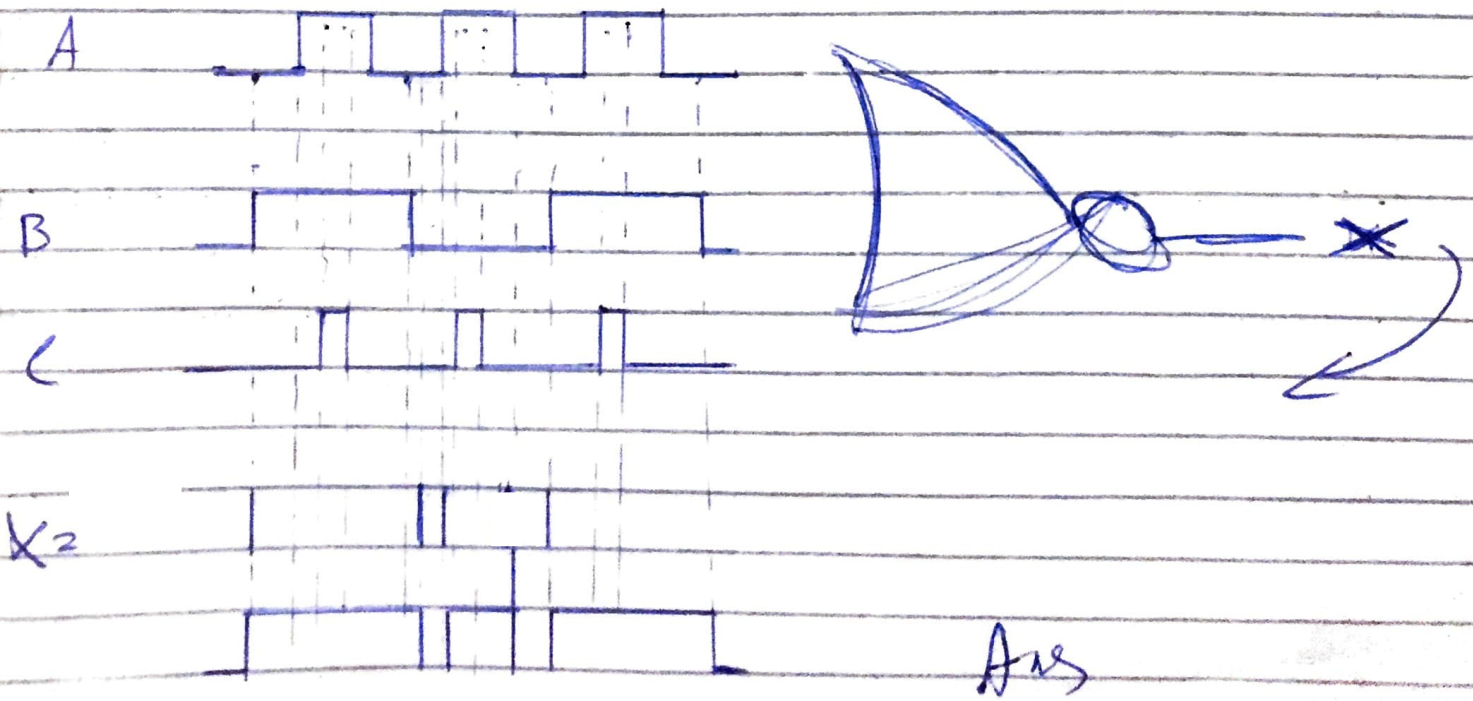


Q8: Determine the output for a two input OR gate when input waveforms are as in figure Q 5. and draw a time diagram.



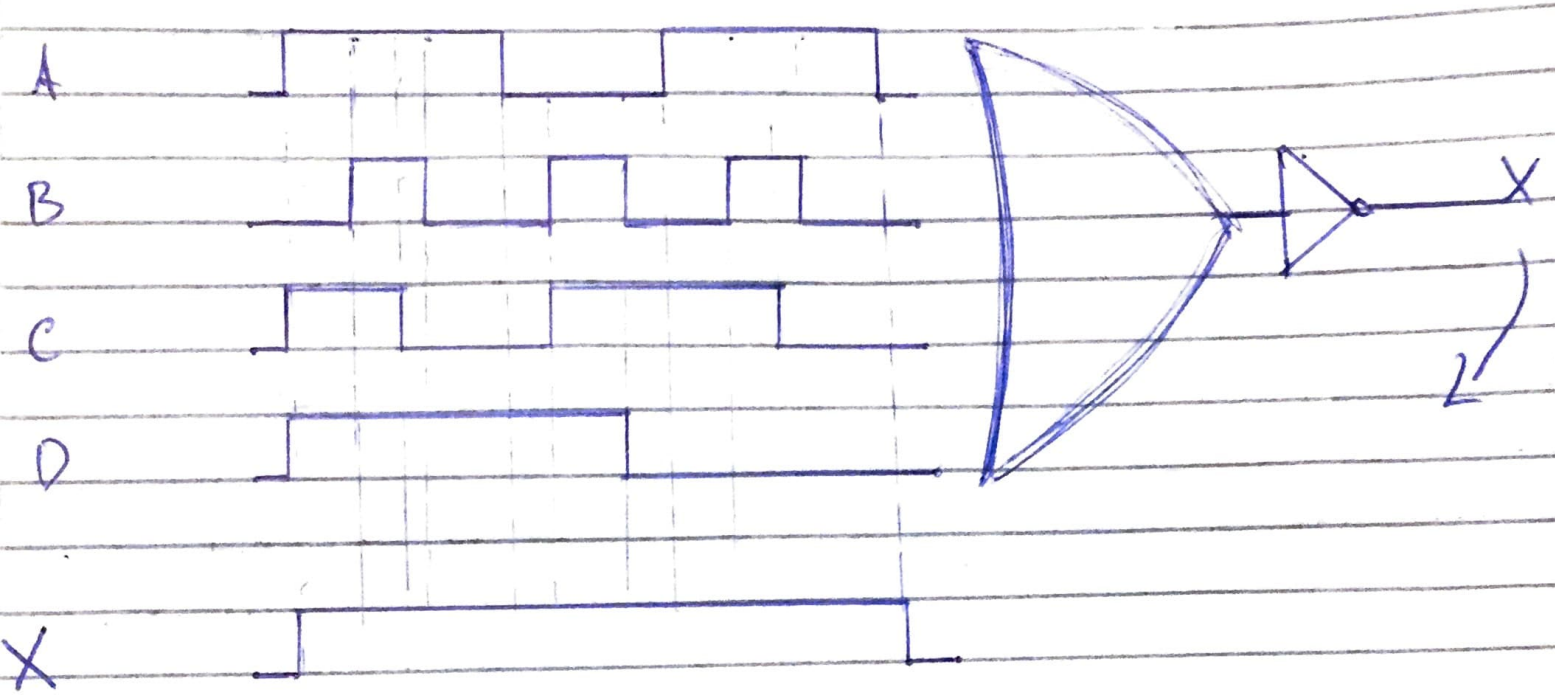
Ans

Q9: Repeat Q.6 for 3 input or gate



Ans

Q10: Repeat Q7 for 4 input OR gate.



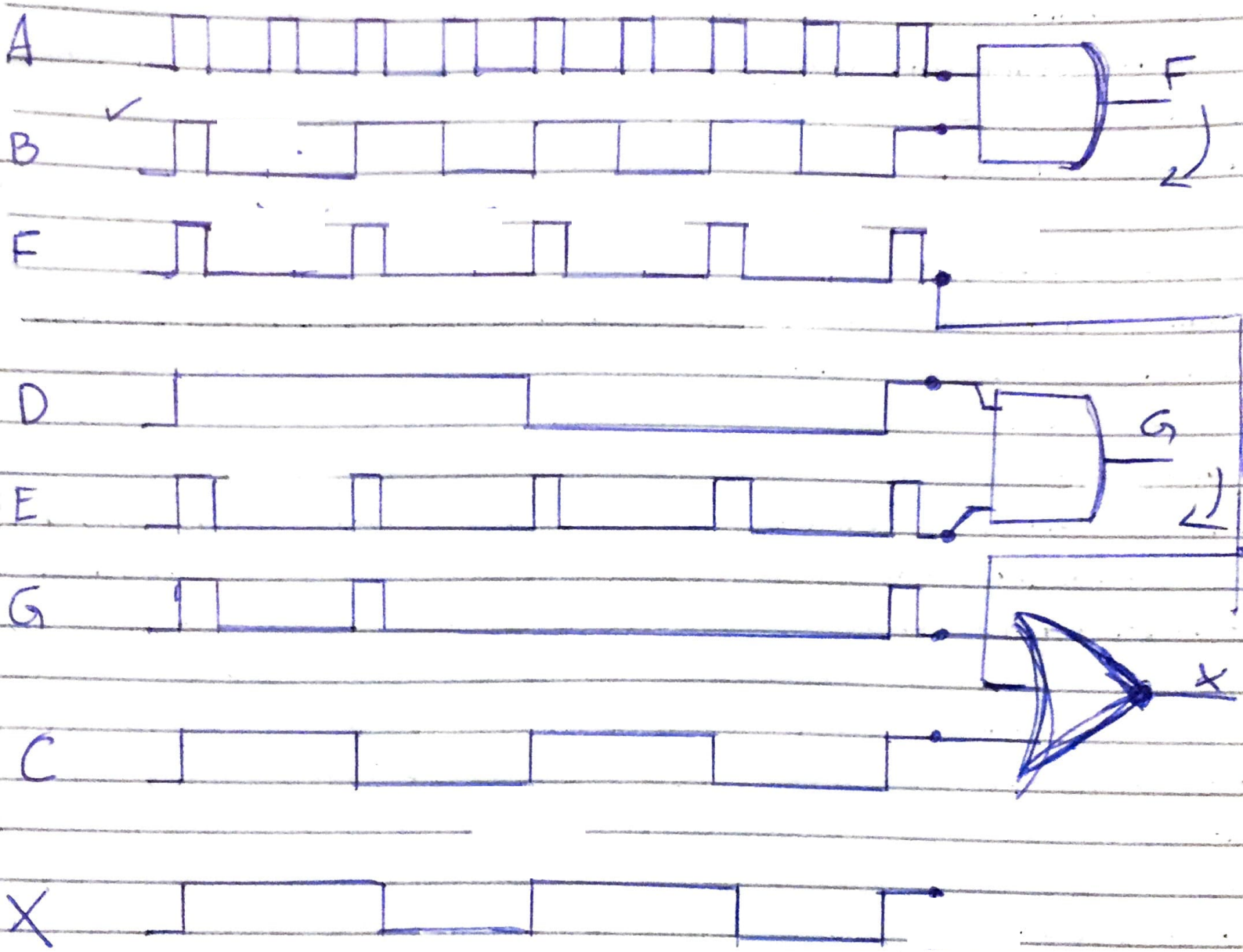
Q11: For the waveforms given in figure, A and B are ANed with output, F, D and E ANed with output G, C, F, and G are ORed, Draw the net output waveform

Sol

$(AB) = F$

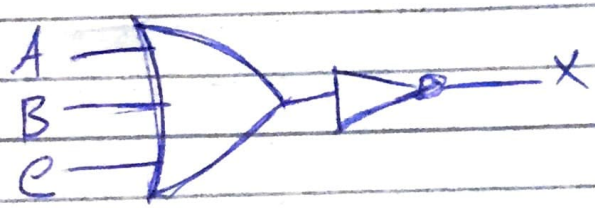
$(DE) = G$

$(C + F + G) = X,$

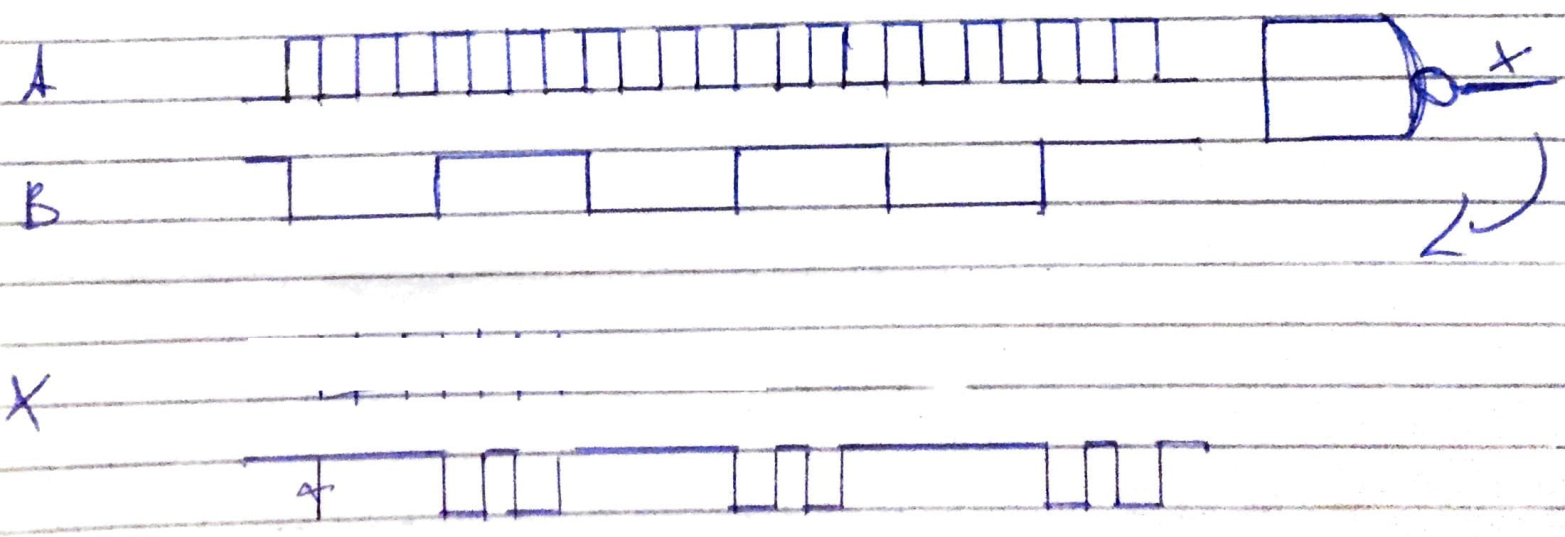

A
B
F
F
D
E
G
G
C
X

Q12: Show the truth table for a system of a 3 input or gate followed by an inverter.

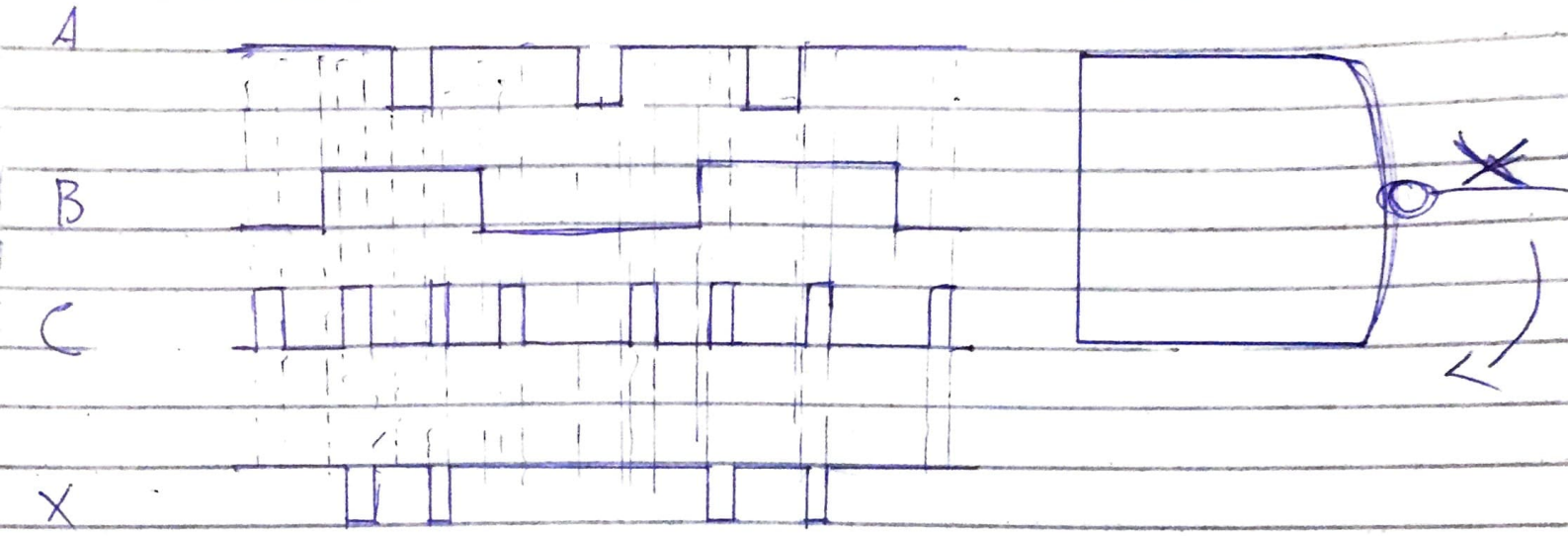
A	B	C	(A+B+C)	$\neg$(A+B+C)
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0



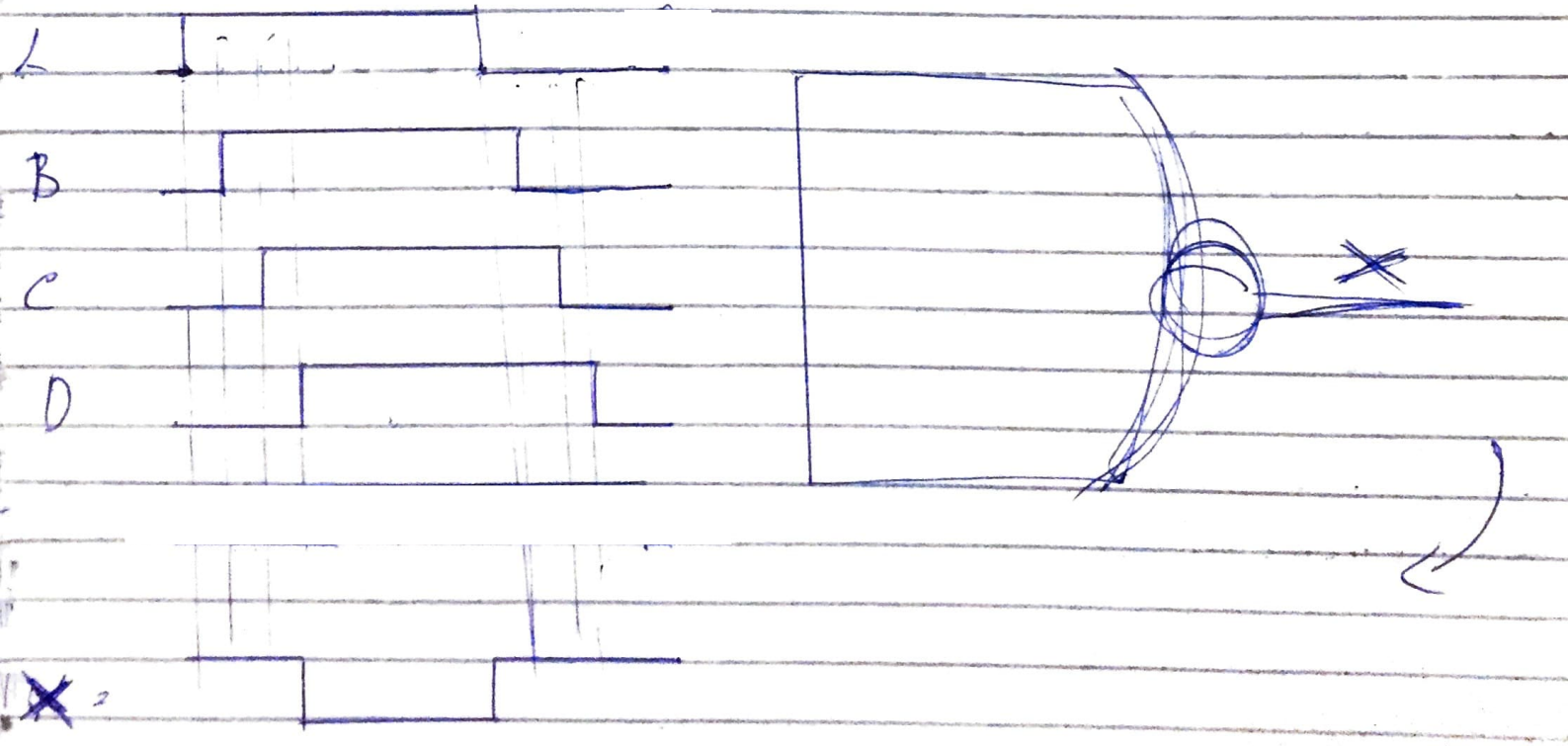
Q13: for the set of input waveforms, Determine the output for the gate shown in the timing diagram.



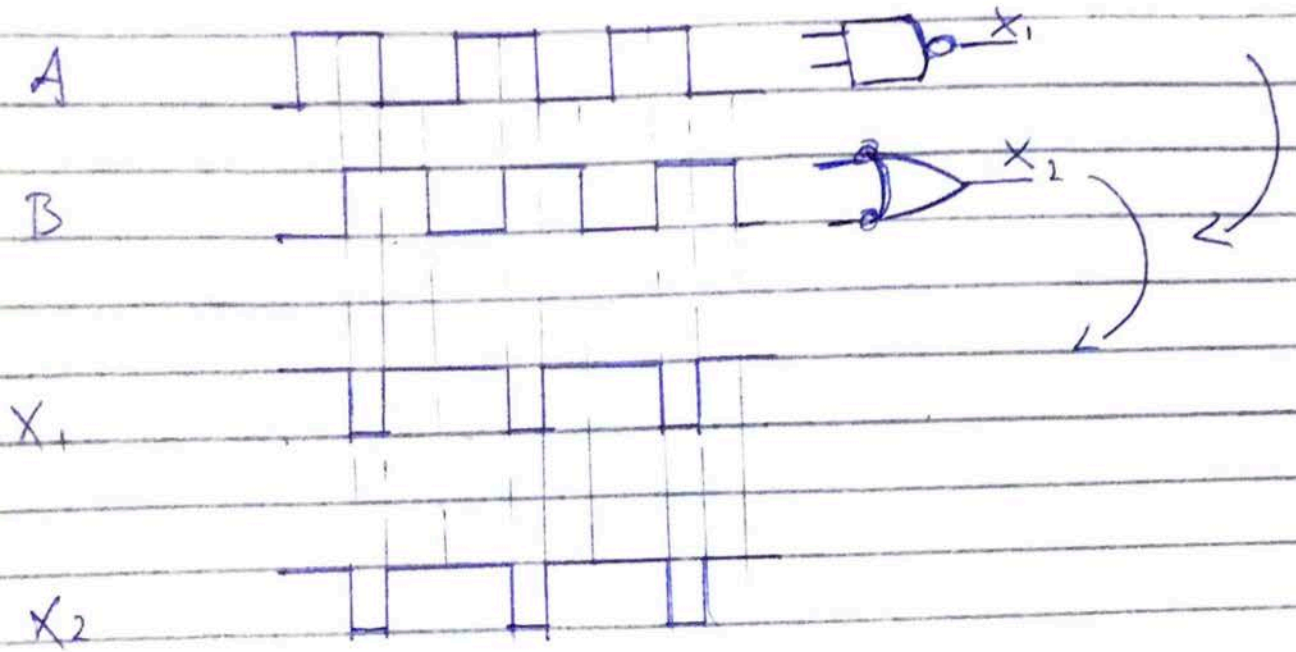
Q14: Determine the gate output for the input waveforms in figure ⊖ and draw the timing diagram.



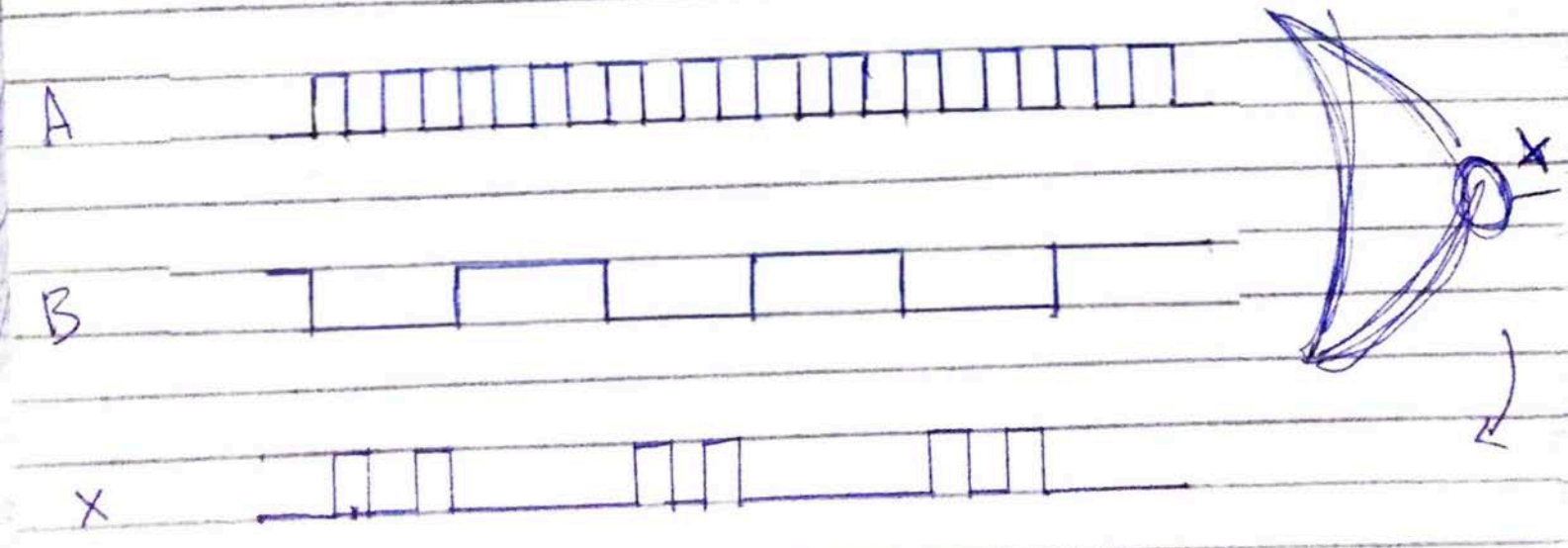
Q15: Determine the output waveform in figure.



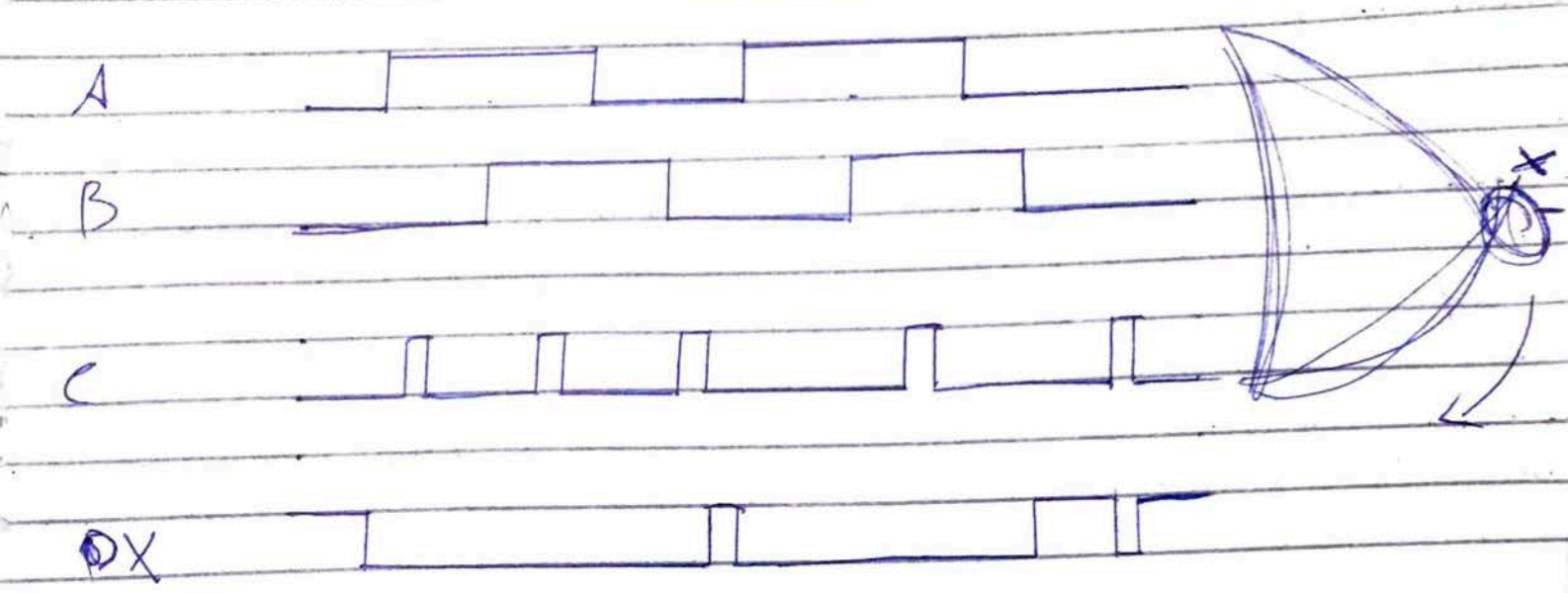
Q16: **The two logic symbols shown in Figure 11 represent equivalent operations. The difference between the two is strictly from a functional viewpoint. For the NAND symbol, look for two HIGHs on the inputs to give a LOW output. For the negative- OR, look for at least one LOW on the inputs to give a HIGH on the output. Using these two functional viewpoints, show that each gate will produce the same output for the given inputs.**



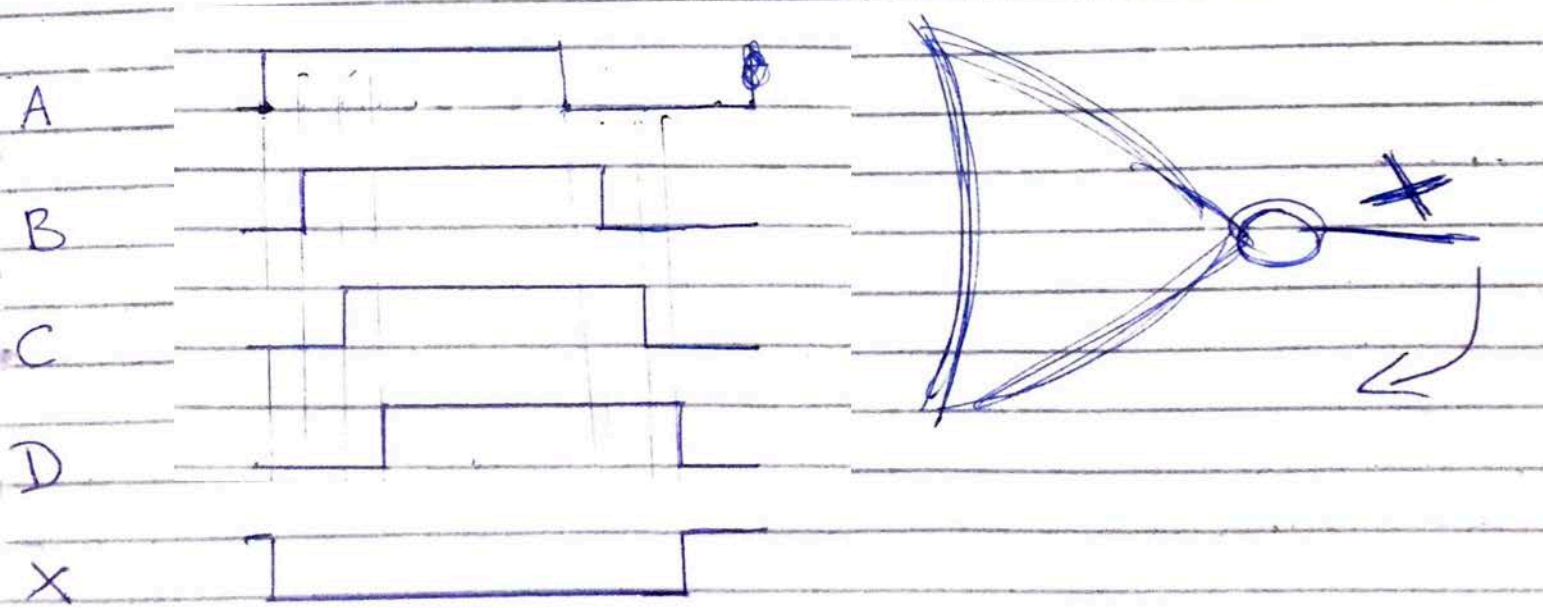
Q17. Repeat Q 13 for 2 input Nor gate.



Q18: Determine the output waveform in figure and draw the timing diagram.

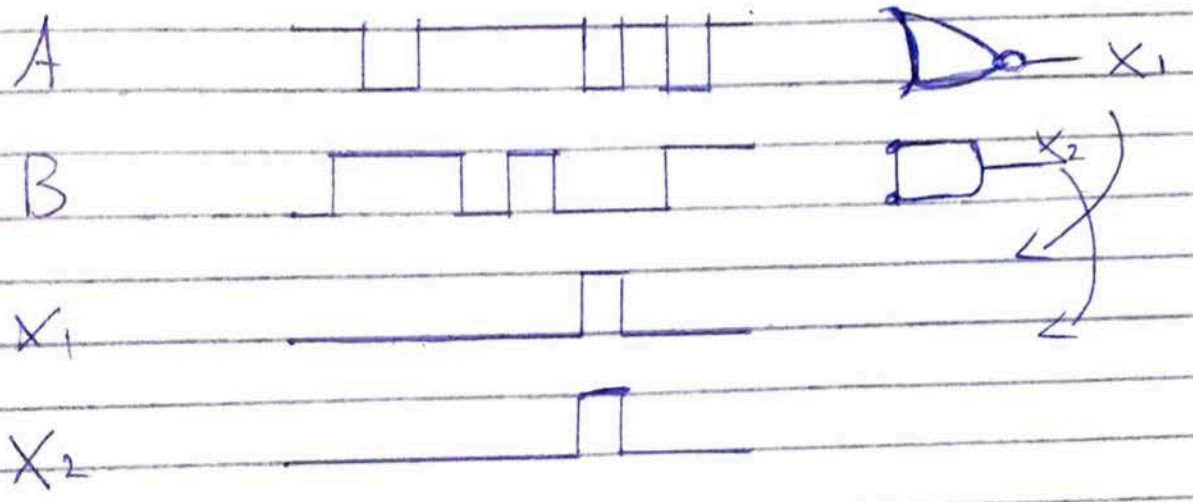


(19) Repeat Q 15 for four input NOR gate.

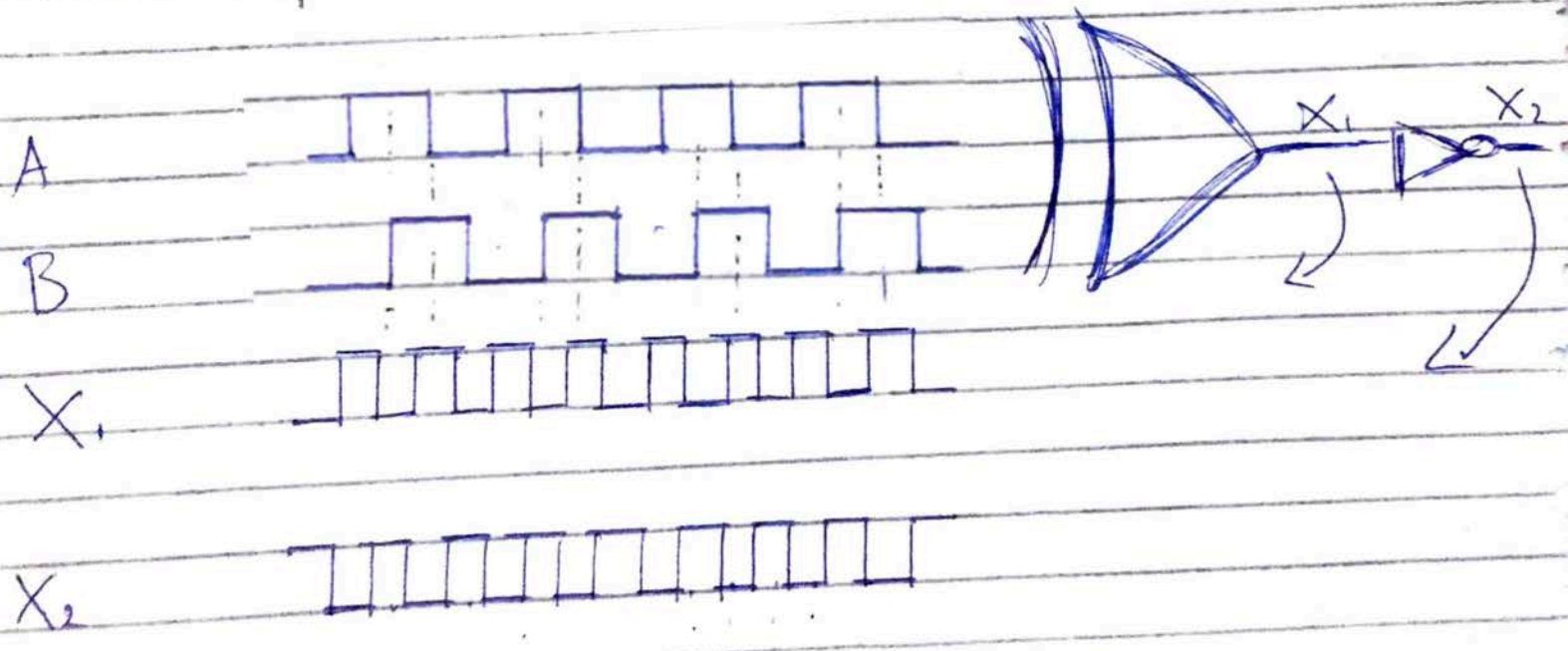


Q 20:

The NOR and the negative-AND symbols represent equivalent operations, but they are functionally different. For the NOR symbol, look for at least one HIGH on the inputs to give a LOW on the output. For the negative-AND, look for two LOWs on the inputs to give a HIGH output. Using these two functional points of view, show that both gates in Figure 12 will produce the same output for the given inputs.



Q21: Repeat Q.5 for Exclusive-OR gate



Q22: Repeat Q5 for 2 exclusive NOR gate