Name	Kazhar Saleem
Id	14455
Assign	1 chap
Sems	4th

Q1 What are four Fuction of comp?

Data processing:

Data may take a wide variety of forms, and the range of processing requirements is broad. RAW data in RAM needs to be processed into useful information, this is performed by the computer processor, also refferred to as the CPU. The CPU together with the computer O.S and the program that's running, takes data and process it.

ii Data storage:

Even if the computer is processing data on the fly, the computer must temporarily stores atleast those piece of data that are being worked on at any given moment. computer perform short term data as well as long-term data storage function.

iii Data movement:

When data are received from a device that are directly connected to the computer, the process is known as input-output, and the device is referred to as a peripheral. When data are moved over longer distances to or from a remote device, the

process is known as data communication control

Within the computer, a control unit manages the computer's resources and orchestrates the performance of its functional parts in response to instructions.

Q. IBM zEnterprise EC12 core layout, explain Function of each sub-area? (1)

i) IFU :- (Instruction Fish Unit)
IFU gets information from memory.

ii) IDU :- Instruction decode Unit :-
The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

iii) LSU :- (Load Store Unit)
The LSU contains the 96 KB L1 data cashet and manages data traffic btw the L2 data cashe and the Functional executional execution Units. Responsible for handling all types of operand accesses.

iv) XU (translation Unit) :-
This Unit translates logical addresses from instructions into physical addresses

in main memory. The XU also contains a translation lookaside buffer (TLB) used to speed up memory access.

v) FXU (Fixed-point Unit):
The FXU executes fixed-point arithmetic operations.

vi) BFU (Binary Floating-point Unit):
The BFU handles all binary and hexa-decimal floating point operations as well as fixed-point multiplication operations.

vii) DFU (decimal Floating point Unit):
The DFU handles both Fixed point and floating point operations on numbers that are stored as decimal digits.

viii) RU (Recovery-Unit):
The RU keeps a copy of the complete state of the system that include all registers, collects hardware fault signals, and manages the hardware recovery actions.

x) cop (dedicated-coprocessor)
The cop is responsible for data compression and encryption functions for each core.

xi) I-cache:
This is a 64-KB L1 instruction cache, allowing the IFU

to Pre-fetch Instructions before they are needed.

L2-control:-

This is the control logic that manages the traffic through the two L2 caches.

Data-L2:-

A 1-MB L2 data cache for all memory traffic other than instruc

Instr-L2:-

A 1-MB L2 instruction cache.

Q3 Discuss the IAS operation?

Ans The IAS operates by respectively performing an instruction cycle as shown in the Fig 1.6 Each instruction cycle consists of two subcycles During the fetch cycle the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR, and MAR. Once the opcode is in the IR the execute cycle is performed.

p.t.o

Execute cycle:

The control circuitry interprets the opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU

d For each of the following examples determine, whether that is an embedded system, explain why or why not?

a: Are program that understand physics and/or hardware embedded?

Ans No, These programs are never considered to be embedded because they are not an integral component of a larger system.

b: Is the internal microprocessor controlling a disk drive is embedded?

Ans Yes, regardless of what the disk drive is used for. The software (Firmware, actually) within the disk drive controls the HDA (head disk assembly) hardware and is hard real time as well.

c: I/O drivers imply that the computer executing the driver is embedded?

Ans No, Input-output drivers do not represent the embedded system.

d: Is a PDA is an embedded sys?
Ans Yes, PDA is an embedded sy? because it is just like a personal computer in hand.

e:- Is the microphone controlling a cell phone an embedded system?
Yes, the Filmware in the cell phone is controlling the radio hardware.

F:- Yes these computers were generally some of the most powerful computer.

g:- If the FMS is not connected to the avionics and is used only for logistic computerization a function readily performed on a laptop the the FMS is clearly nonembedded.

H. Yes both in the Simulator and in the thing being tested in the HIL Simulator.

i. Yes in this case of the "system" is the combination of the pacemaker and the person's heart.

j. Yes it is part of a large system, the engine, and it is directly monitoring and controlling the engine through special hardware.

Main structural components of computer?
There are four main structural components:
central processing unit (CPU): controls the operation of the computer and performs its data processing functions often simply referred to as processor.
Main memory: stores data
I/O: Moves data b/w the computer and its external environment
System interconnection:
Some mechanism that provides for communication among CPU, main memory and I/O.

Key characteristics of a planned computer family?
similar or identical instr set: In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family, this means that program can move up but not down.

Similar or identical O.S:- The same basic o.s is availble for all family members.

Increasing speed: The rate of instruction execution increase in going from lower to higher family members.

Increasing no of I/O ports: The number of I/O ports increase in going from lower to higher family members.

Increasing memory size: The size of main memory increases in going from lower to higher family members.

Increasing cost: At a given point in time, the cost of a system increases in go iu from lower to higher family members.

Stored program computer?

A fundamental design approach first implement in the IAS computer is known as the stored program concept. This idea is usually attributed to the mathematician John von Neumann.

The first publication of the idea was in a 1945 proposal by von Neumann for a new

computer, The EDVAC (Electronic discrete variable computer)

An 1946, von Neumann and his colleagues began the design of a new stored-program computer, refferred to as the IAS compuler at the princeton institute for Advanced Studies

It consist of:

main memory: which stores both data and instructions.

ALU :- capable of operation on binary data.

Moore's law?

The famous moore's law which was propounded by gordon Moore, co founder of intel in 1965 [MOOR 65]. Moore observed that the number of transistors that could be put on a single chip was doubling every year.

The pace slowed to a doubling year 18 months in the 1970s but has sustained that rate over since.

The consequences of Moore's law are profound:

1. The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2. Because logic and memory elements are placed closer together on more densely packed chips the electrical path length is shortened increasing operating speed.
3. The computer becomes smaller, making it more convenient to place in a variety of environments.
4. There is a reduction in power requirements.
5. With more circuitry on each chip there are fewer interchip connections.

Computer organization and Architecture?

Computer Architecture	comp. Organization.
Computer Architecture is concerned with the way hardware components are connected together to form a computer System.	Computer organization is concerned with the structure and behavior of a computer system as seen by the user.
It acts as the interface b/w hardware and software.	It deals with the components of a connection in a system.
While designing a comp. Archi is considered first	An organization is done on the basis of Architecture
CA deals with high level design issue.	CO deals with low level - design issues

RISC and CISC

Basis for comparison	RISC	CISC
Emphasis on	Software	Hardware
Includes	Single clock	Multi-clock
Instruction set size	small	Large
Instr format	Fixed 32 bit	Varying formats (16-64)
clock rate	50-150MHz	33-50 MHz
cpu control	Hardwired without control memory	Microcoded using control memory (ROM)

C Microprocessors or Microcontrollers?

* Microprocessors is an IC which has only the CPU inside them i.e only the processing powers such as Intel pentium 1, 2, 3, 4 core 2 duo etc.

* Microcontroller has a CPU, in addition with a fixed amount of RAM, ROM and other peripherals all embedded on a single chip.

D

	Cortex A	Cortex R	Cortex M
①	Application processors	Real time processors	Micro-controllers
②	High performance and efficiency	High performance	low-performance
③	Applications mobiles, tablet	Applications- medical devices car system	Application robotic System
④	It is connected to large amount of memory	—	It is connected to less memory.
⑤	Runs at high clock frequency	It turns on high clock frequency	It runs at clock speed

Contents are divided up into two 5 bit instructions LH and RH

LH instruction = 0 10FA

opcode = 01

address = 0FA

RH instruction = 210FB

Opcode = 21

address = 0FB

Since this is in the hexadecimal form you have to convert the numbers to binary form (use the SAS instruction set).

LH instructions:
01 = 00000001 = Load M(X)
M(X) refers to the memory address location 0FA.
The first 5 bits of 08A should read - LOAD M1(0FA).
RH instructions:
21 = 00100001 = STOR M1(X)
M1(X) refers to the memory address location 0FB
The second 5 bits of 08A should read - STOR M(0FB)
Finally the assembly language code for 08A 010FA210FB is
LOAD M1(0FA)
STOR M1(0FB)

2 Here is a simple way to Understand this problem:
Contents are divided up into two 5 bit instruction LH and RH
LH instruction = 010FA
opcode = 01
address = 0FA
RH instruction = 0F08D
opcode = 0F
address = 08D

Since this is in hexadecimal form you have to convert the numbers to binary form: (use 9AS instr set)

LH instruction:

01 = 00000001 = LOAD M(X)

M(X) refers to the memory address location OFA.

The first 5 bits of 08B should read - LOAD M(OFA)

RH instruction:

OF = 00001111 = JUMP + M(X, 0:19)

refers to the memory address location 08D.

The second 5 bits of 08B should read - JUMP + M(08D, 0:19)

Finally the assembly language code for 08B 010FA 0F08D is

LOAD M(OFA)

JUMP + M(08D, 0:19)

Contents are divided up into two 5 bit instructions LH and RH

LH instruction = 020FA

opcode = 02

address = OFA

RH instruction = 210FB

opcode = 21

address = OFB

convert hexadecimal to binary form.
LH instructions:
02 = 00000010 = LOAD - M(X)
M(X) refers to the memory address location OFA.
The first 5 bits of 08C should read - LOAD - M(OFA)
RH instructions:
21 = 00100001 = STOR M(X)
M(X) refers to the memory address location OFB.
The second 5 bits of 08C should read - STOR M(OFB)
Finally the assembly language code for 08C 020FA210FB is
LOAD - M(OFA)
STOR M(OFB)

b Explain what it does?

① An 08A address, the M(OFA) transfer to the accumulator and transfer contents of accumulator to memory location OFB.

② An 08B address the M(OFA) transfer to the accumulator and take next instruction from left half of M(08D).

3 An 08C address the - M(0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB.