Name : Sajawal Khan

Department: Computer Science

ID : 14756

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Submitted to: Sir Amin

Q= Give detail answer to each of the following.

(a) Discuss different types of Semi-conductor memories in detail.

There are various types of Semi-conductor memories. The most common is refered to as RAM (random access memory). Most type have the property of random Access memory which means that it takes the same amount of time to access any memory location.

* Here is a table of Semi-conductor memory types.

| Memory types | Category | Erasure | Write mechanism | Volatility |
|---|---|---|---|---|
| RAM (random memory) | Read/write memory | Electrically Bite level | Electrically | volatile |
| ROM | Readonly memory | Not posible | Masks | |
| PROM | | to right | | |
| EPROM | | chip level | | |
| EEPROM | Read most memory | electrically at level | | Non |
| Flash memory | | electrically block level | Electri-cally | volatile |

(b) Explain the read & write operation for the SRAM Cell Using diagram

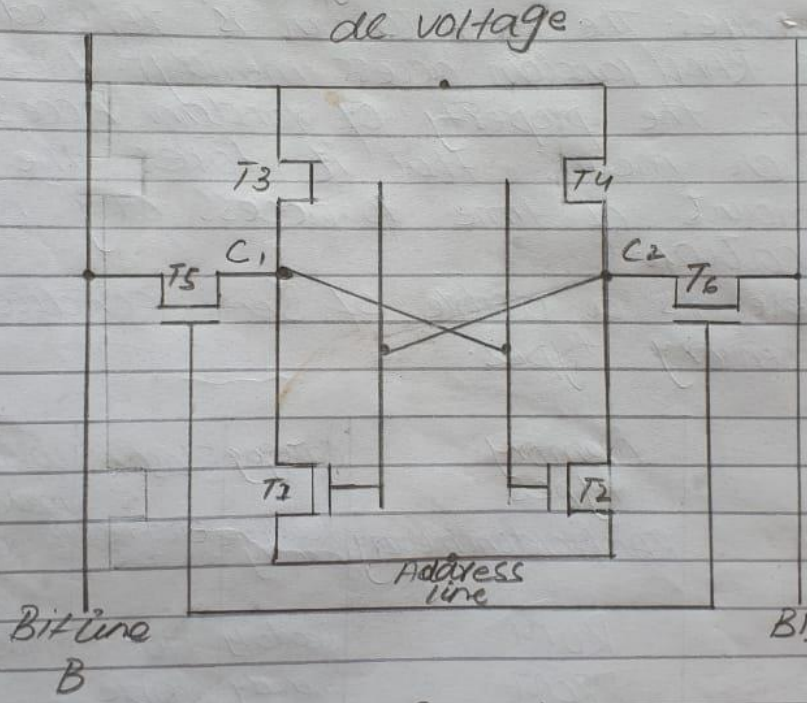
* Read operation

(3)

In SRAM for only operation to be performed the word line should be high. To perform read operation intially

* Write operation:-

Consider the memory bits consist of Q=0 & Q=1




(b) Static ram (SRAM) cell

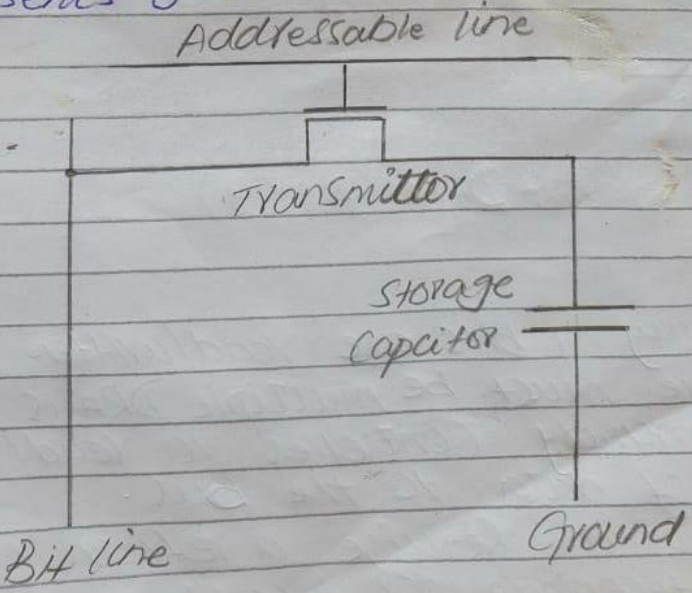
(C) Explain the read & write operation for the DRAM cell using diagram

Read operation:-

When the address line is selected the transistor turn on & the charge stored on the capcitor is fed out onto a bit line & to a sense complifier. it compare the capcitor voltage to a reference value & determine if the cell contains a logic 1 or a logic 0.

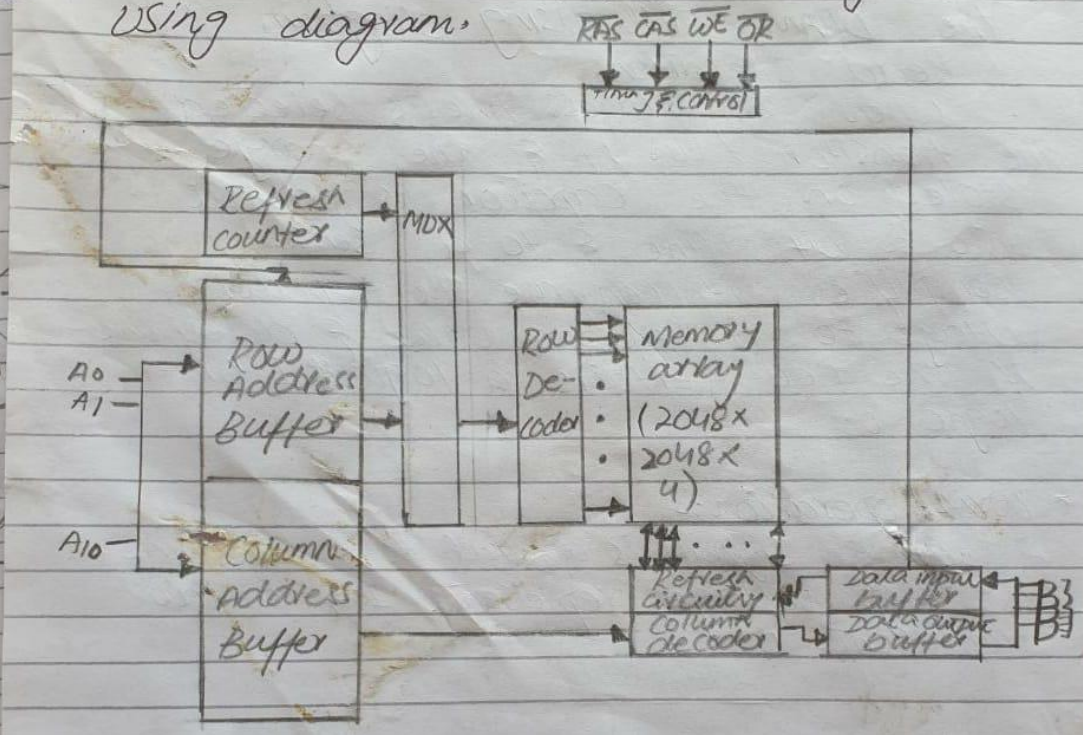
* Write operation:-

A voltage signal is applied to a bit line, a high voltage represents 1 & a low represents 0



(4)

(d) Discuss 16-Mbit DRAM (4M×4) organization using diagram.



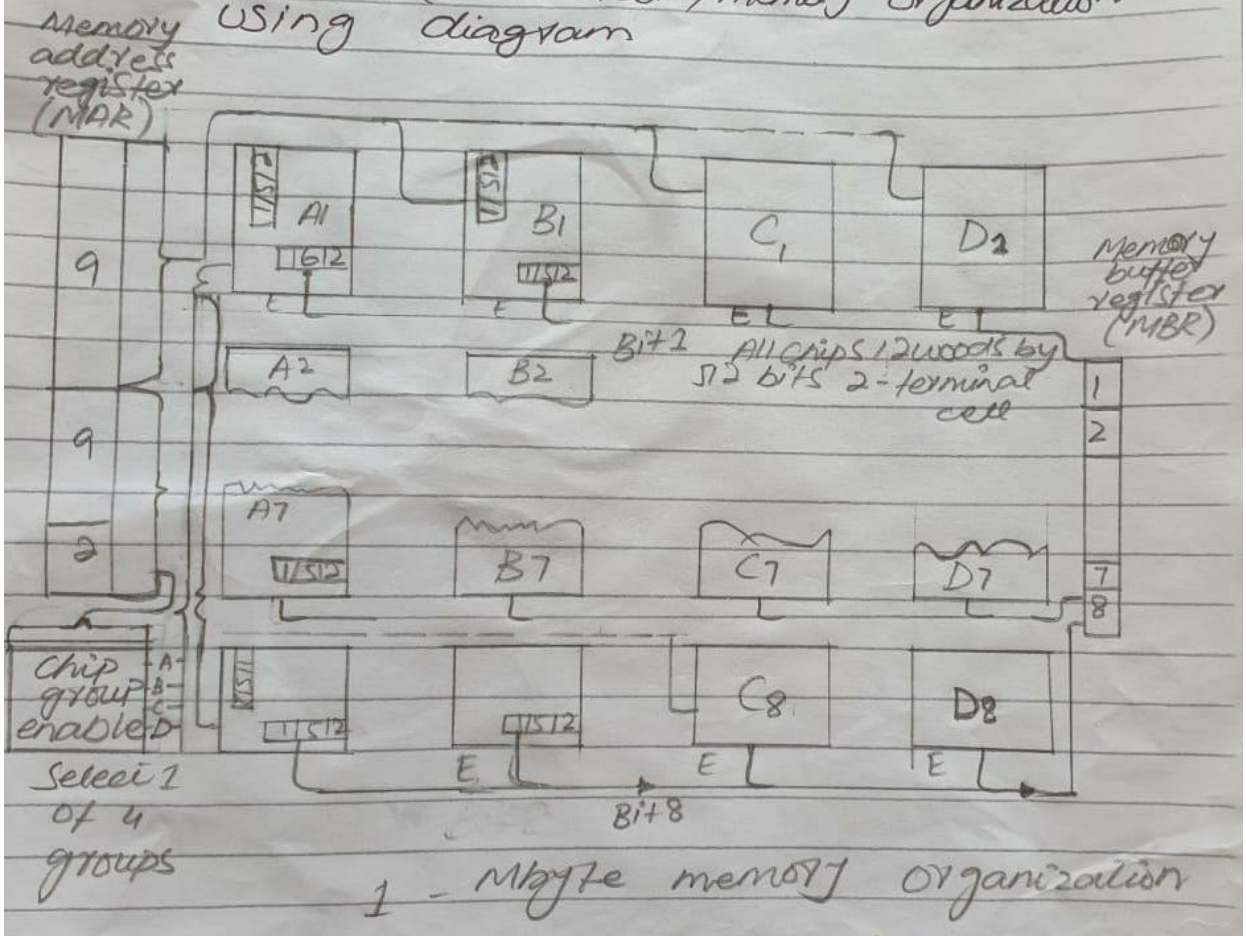

Typical Megabit DRAM (4M×4)

Because only 4 bits are read/written to their DRAM, there must be multiple DRAMs connected to the memory controller to read/written a word of data to the bus.

All the DRAMs require a refresh operation A simple technique for refreshing is in effect to disable the DRAM chip while all data

cells are refreshed. The refresh counter steps through all of the row values. This causes each cell in row to be refresh

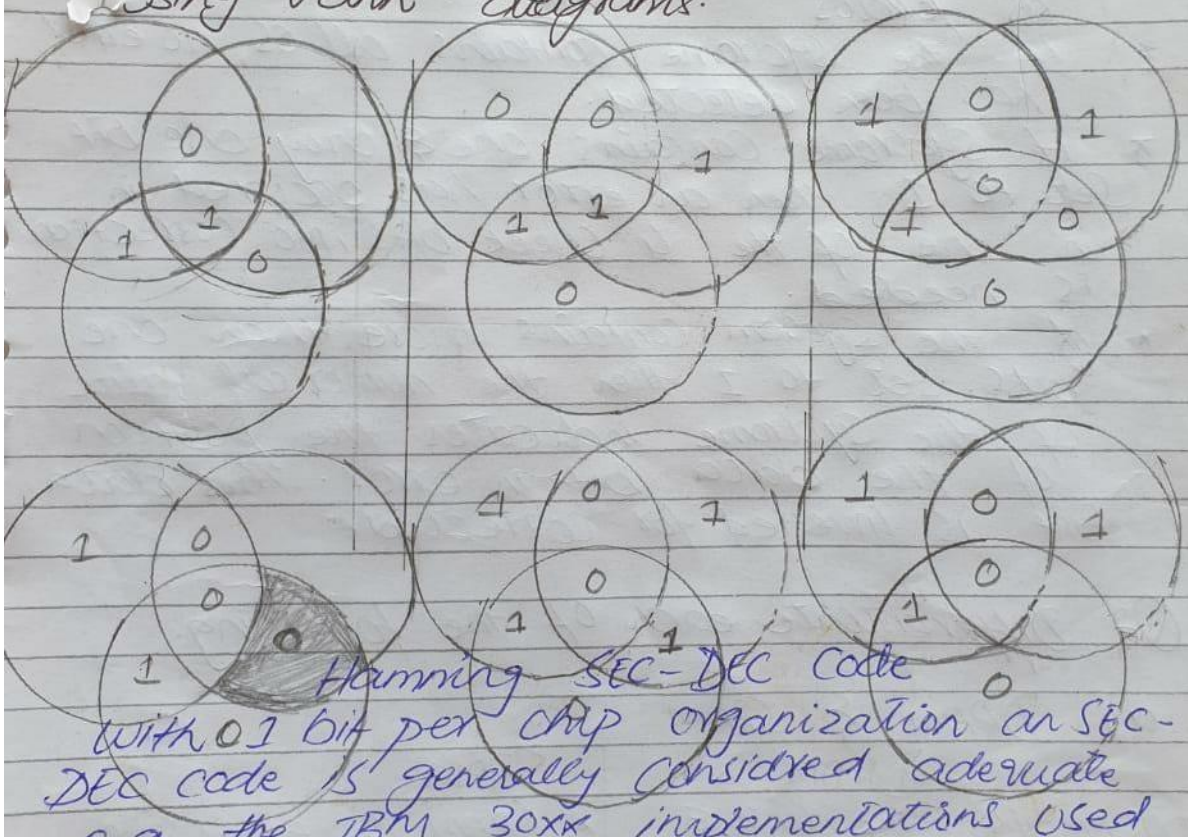
c) Discuss 2MB (256k x 4x 8Bit) memory organization using diagram




1 - Mbyte memory organization

The possible organization is secured of a memory consisting of 1M word by 8 bits per word. In this case we have four columns of chips, each column containing 256K words arranged.

(f) Explain Hamming SEC-DEC code using venn diagrams.



Hamming SEC-DEC code with 01 bit per chip organization an SEC-DEC code is generally considered adequate e.g the IBM 30xx implementations used an 8 bits SEC-DEC code for each 64 bits of data in main memory. The size of main memory is actually about 12% larger than is apperent to the user

| | |
|---|---|
| * DRAM are normal in Speed<br>* SRAM is used for cache memory | * DRAM is used for main memory. |

b) EEPROM & flash memory.

| EEPROM | Flash memory |
|---|---|
| * EEPROM devices can erase any byte of memory at any time.<br>* EEPROM uses NOR type memory<br>* EEPROM is byte-wise erasable | * Flash memory can only erase an entire chunk, or "sector" of memory at a time.<br>* Flash memory uses Nand type memory<br>* Flash is block-wise erasable. |

QNO #3

$M = 8$

$2^K - 1 >= K + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

* The check bits are in bit numbers 1, 2, 4 & 8
* Check bit 8 calculated by values in bit numbers: 9, 10, 11 & 12.
* Check bit 4 calculated by values in bit numbers: 5, 6, 7 & 12
* Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 & 11
* Check bit 1 calculated by values in bit numbers: 3, 5, 7, 9, 10 & 11

This the check bits are: 1011