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Assignment NO1

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Q:NO:01

Ans:

A:

Desktop Applications:

* Image proccessing
* Speech ragonization

* Simulation modeling.
* Voice and video connection
* Video conferencing.
* Multimedia.
* Three dimensional rendering

B:

=> Pipelining: It enable processor to work simultaneously on multiple instruction.

=> Branch prediction: It increase the amount of work available for processor to execute.

=> Superscale Execution: The ability to use more than one instruction in every clock cycle.

=> Data flow analysis:

Processor creates optimized schedule for data dependent on each other

=> Speculative execution:

Enables processor to keep its execution engine as busy as possible.

E:

Power:

As the density and clock speed on chip increase. The power density also increases. The heat generated on high density, Speed is becoming a serier issue.

RC delay:

The speed of electron flow decreases by the capacitance and resistance by metal wires. Delay increases as RC product increases.

Memory Latency and throughput:

Latency and throughput lay processor speed.

D:

A program running on a single processor such that a fraction of execution time involves code that is inherently super sequential and a fraction that is parallaligable.

Let T be time for execution of single processor

(6)

N be number of processors. Speed up be

$$\text{Speed up} = \frac{\text{Time to execute on Single processor}}{\text{Time to execute on N processor.}}$$

$$= \frac{T(1-f) + Tf}{T(1-f) + \frac{Tf}{N}}$$

$$\text{Speed up} = \frac{1}{1-f+\frac{f}{N}}$$

(E):

Multicore: A computer processor integrated circuit with two or more separated processor units called cores, each of cores which read and execute program instruction, as if computer had several processors.

At increase speed without increasing clock rate.

Mic:

The development of Software to exploit a large number of core led to the introduction of Mic (Many integrated Core)

Originally Intel effort in this direction was Larrabee and was late to market. Instead it was turned into Compute-dedicated chip.

A homogenous collection of general processors on a chip.

GPU:

A Gpu is design for graphical data.

It is used for 2D 3D rendering and encoding it perform parallel operations on multiple sets of data.
Gpu's are increasing in use for game graphics designing etc.

Q:NO:02:
Ans:
A:

CPI:

$$CPI = (1 \times 46000) + (2 \times 23000) + (2 \times 16000) + (2 \times 9000)/100$$

$$CPI = 162000/100$$

$$\boxed{CPI = 1620}$$

MIPS Rate:

$$MIPS\ Rate = 60\ MHz / 1620 \times 10^6$$

$$= 60 \times 10^6\ Hz / 1620 \times 10^6$$

$$= 60\ Hz / 1620$$

$$\boxed{MIPS\ Rate = 0.037}$$

Execution time:

$$T = Ic / (MIPS \times 10^6)$$

$$T = 109000 / 37 \times 10^3$$

$$T = 2.811\ sec$$

(9)

(B)

For Machine A:

$$CPI = (1 \times 8 + 3 \times 4 + 4 \times 2 + 3 \times 4) \times 10^6 / (8+4+2+4) \times 10^6$$

$$CPI = 40 \times 10^6 / 18 \times 10^6$$

$$\underline{CPI = 2.22}$$

$$MIPS = 200\,Mhz / 2.22 \times 10^6$$

$$\underline{MIPS = 90}$$

$$T = 18 \times 10^6 / 90 \times 10^6$$

$$\underline{T = 0.2\ Sec}$$

(16)

Machine B:

$CPI = (1\times10 + 2\times8 + 4\times2 + 3\times4) \times 10^6 / (10+8+2+4)\times10^6$

$CPI = 46/42$

$CPI = 1.92$

$MIPS = 200\,10^6 / 1.96\times10^6$

$MIPS = 104$

$T = 24\times10^6 / 104\times10^6$

$T = 0.23$ sec

(C)

a: $MIPS = IC/T\times10^6$

$IC = MIPS \times T\times10^6$

$18\times1\times10^6 / 1\times12\times10^6$

$= 18/12$

$= 1.5$

b:

Vax 11/780 CPI =

$(5\ MHz) / (1 \times 10^6) = \underline{5}$

IBM RS/6000 CPI =

$(25\ MHz) / (18 \times 10^6) = \underline{1.4}$

D:

(a) Since we have Same Instruction set mix means additional Instruction could be accomulated between instruction types

Graph:

Instruction Type	CPI	Instruction Mix
Arithmatic Logic	1	60%
Load / Store cache hit	2	18%
Branch	4	12%
Memory ref cache miss	12	10%

(13.)

Average cpi = (1 × 0.6) + (2 × 0.18)
+ (4 × 0.12) + (12 × 0.1)

CPI = 2.64

(b) MIPS = 400 / 2.64

MIPS = 152

(c)

Execution time for one processor

$T = Ic / (MIPS \times 10^6)$

$T = (2 \times 10^6) / (178 \times 10^6)$

$T_1 = 11$ ms

For 8 processors

$T_8 = \dfrac{2 \times 10^6 / 8 + 0.25}{152 \times 10^6}$

$T_8 = 1.8$ ms

So;

Speed up = Time for Single processor execution / Time for n processors

Speed up = 11 / 1.8

Speedup = 6.11

(d) From given information it is not obivous how to quantify this effect in Amdahl's equation.
So suppose fraction of code which is parallelizable is F = 1

Amdahl's law observed
Speedup = N = 8
Then the actual speed is 75% to that of theoratical speed