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Subj DSD

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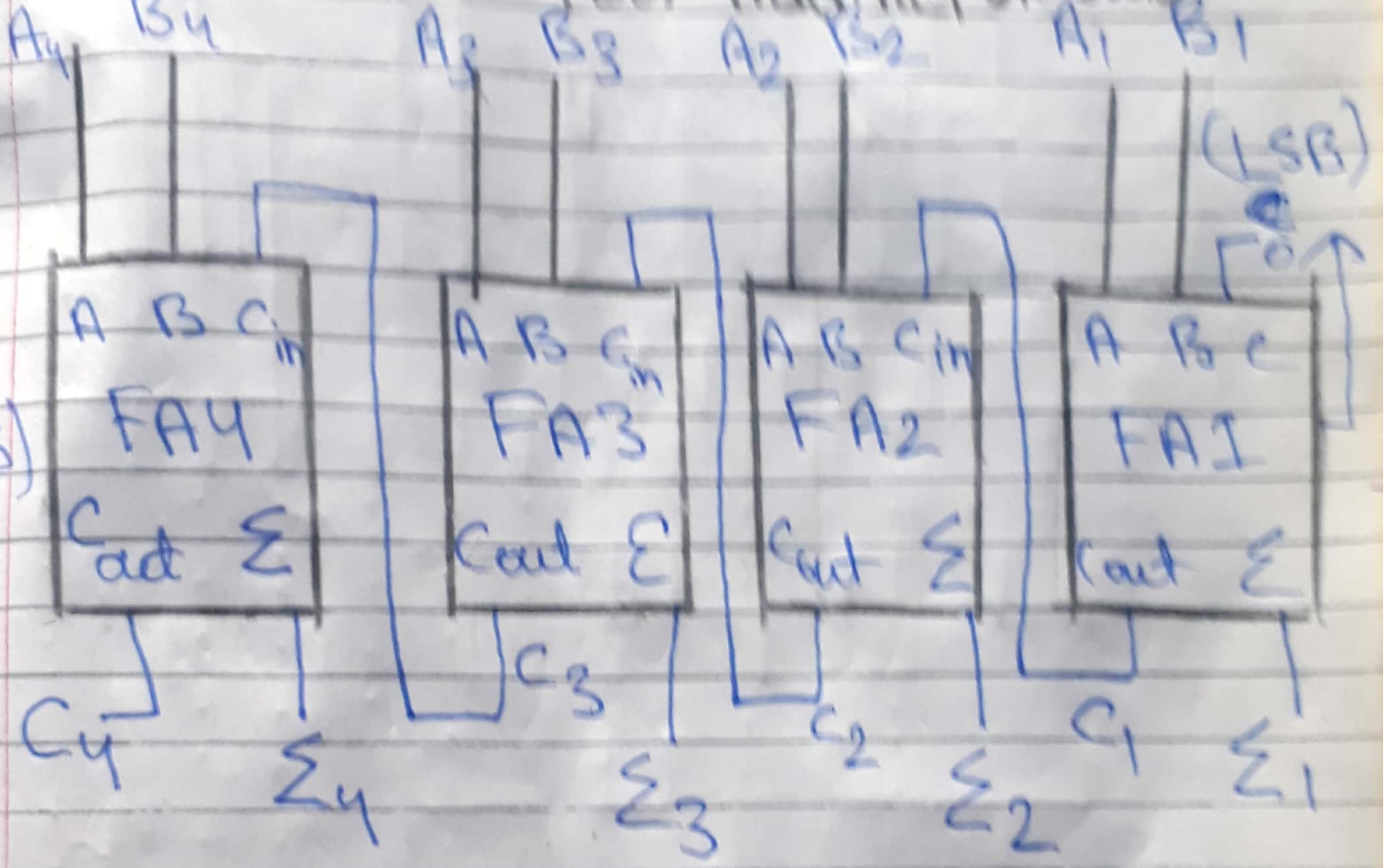
BS (S/E)

Semister : 9th

final TERM Paper

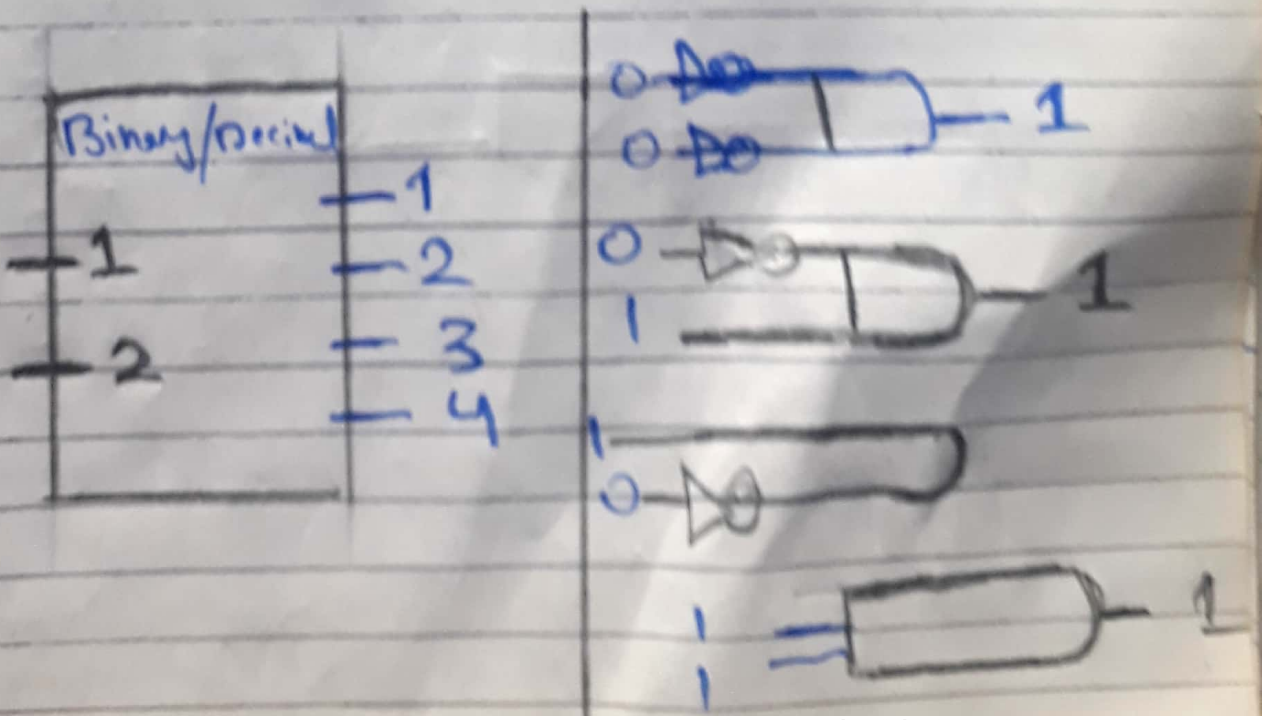
(Q1)

(a) A circuit for Adding or Subtwo 4 bit



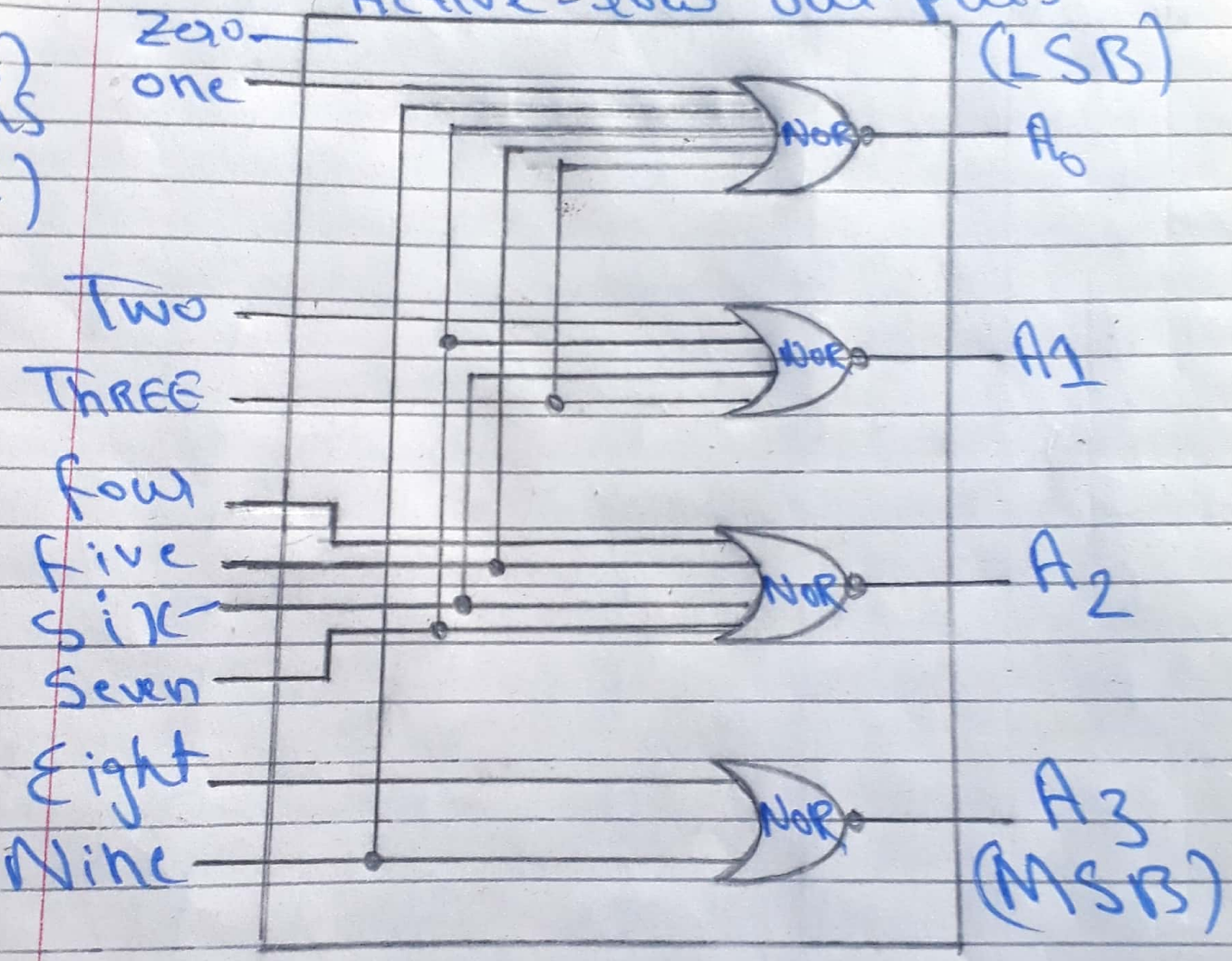
Q1 4-bit active low decoder.

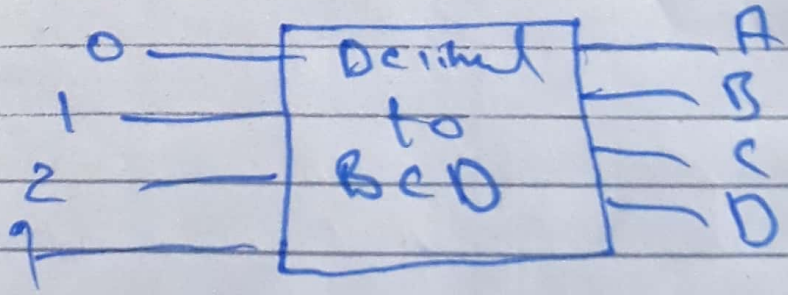
(b)



Q1 (c) Decimal to BCD Encoder. (2)

Active-high inputs
Active-low outputs





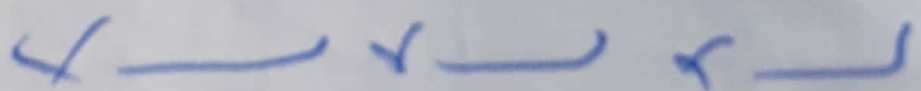
Ans (c)

P.T.O

(3)

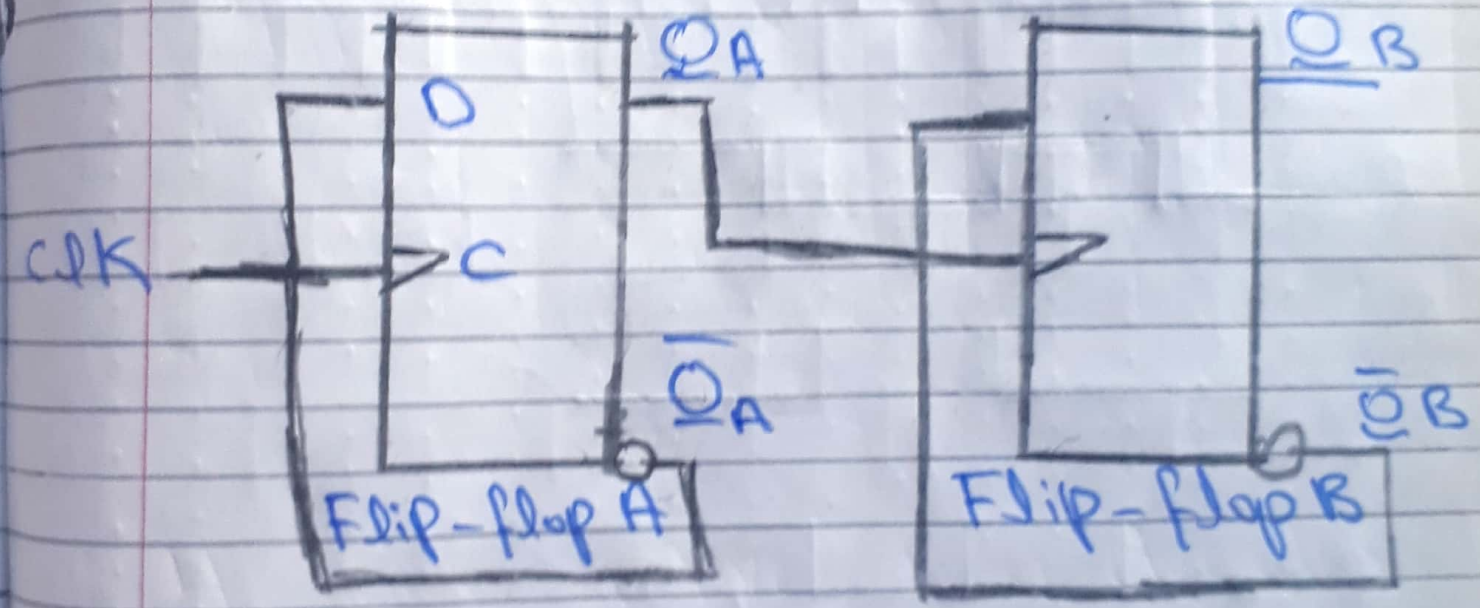
Decimal to BCD encoder

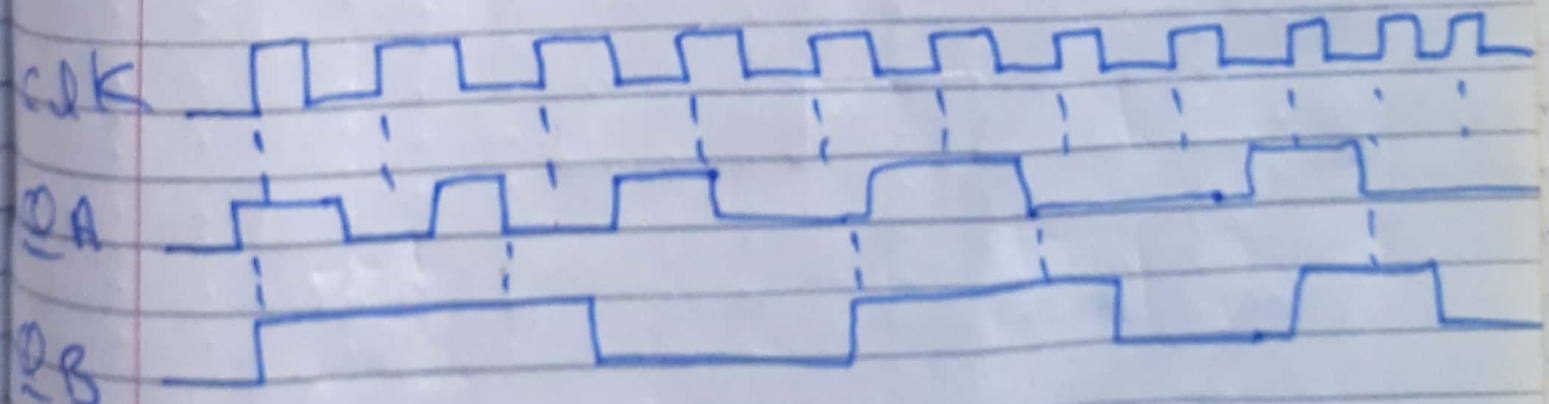
Input	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



Q1

d) Frequency divider (use 3 J-K flip flops and assum 16 KHz of the intial wave form.



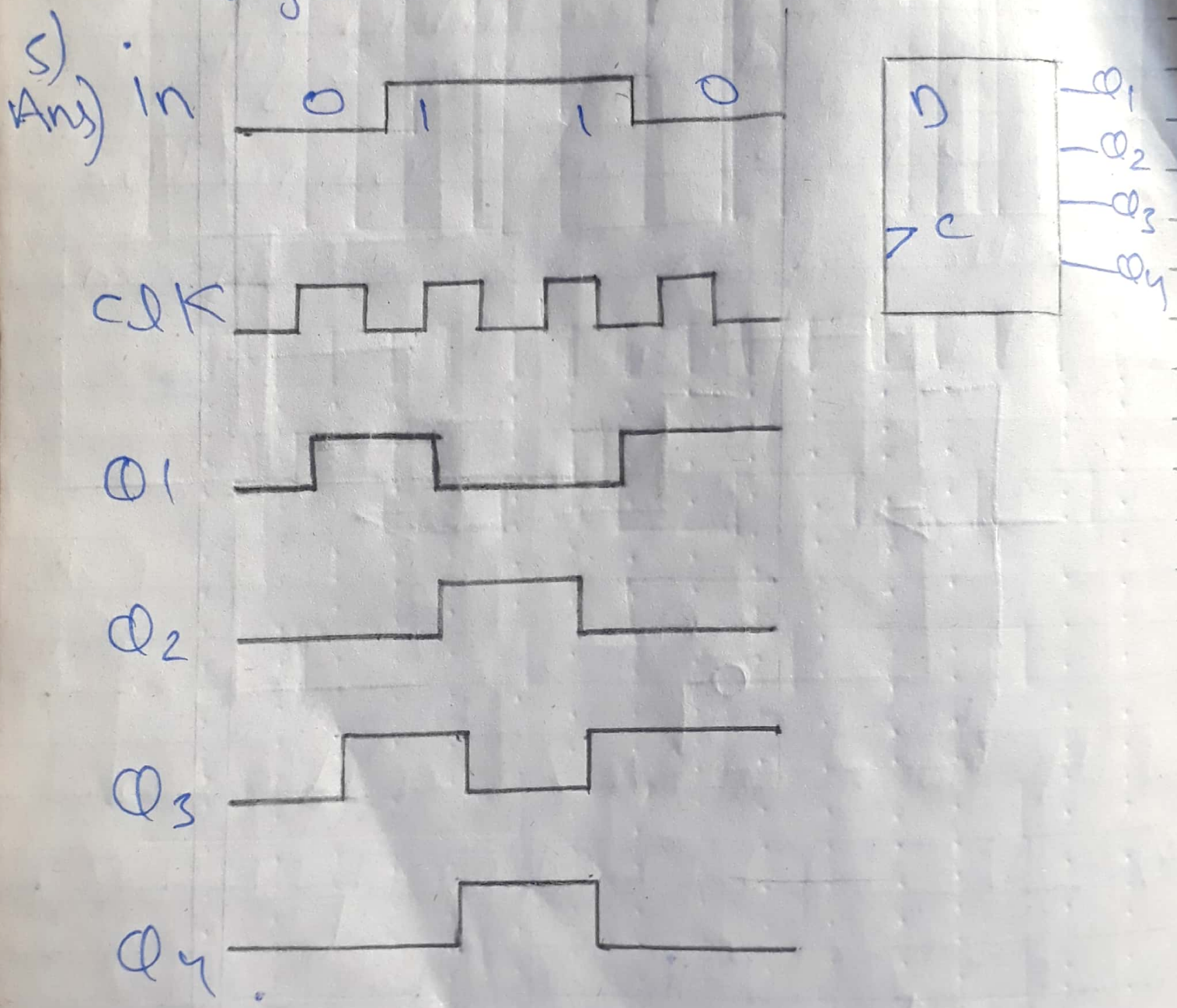


So here is the frequency divader

(8) (5)

Q5) use the waveform. outputs (Q_1, Q_2, Q_3, Q_4) for the shift register. Assume they are cleared

Ans)

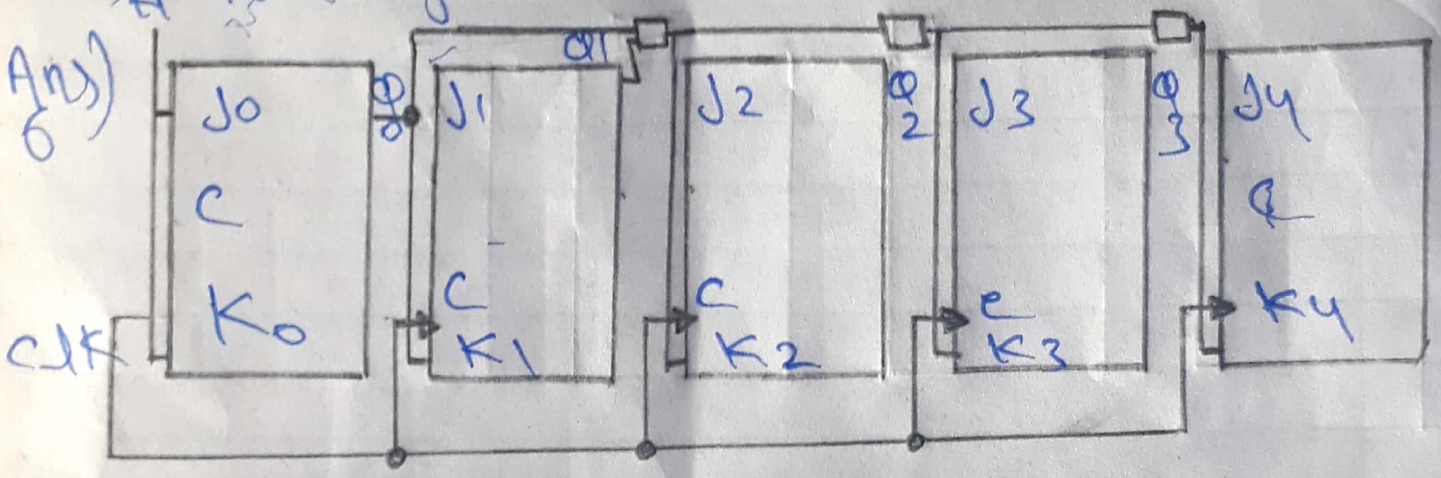


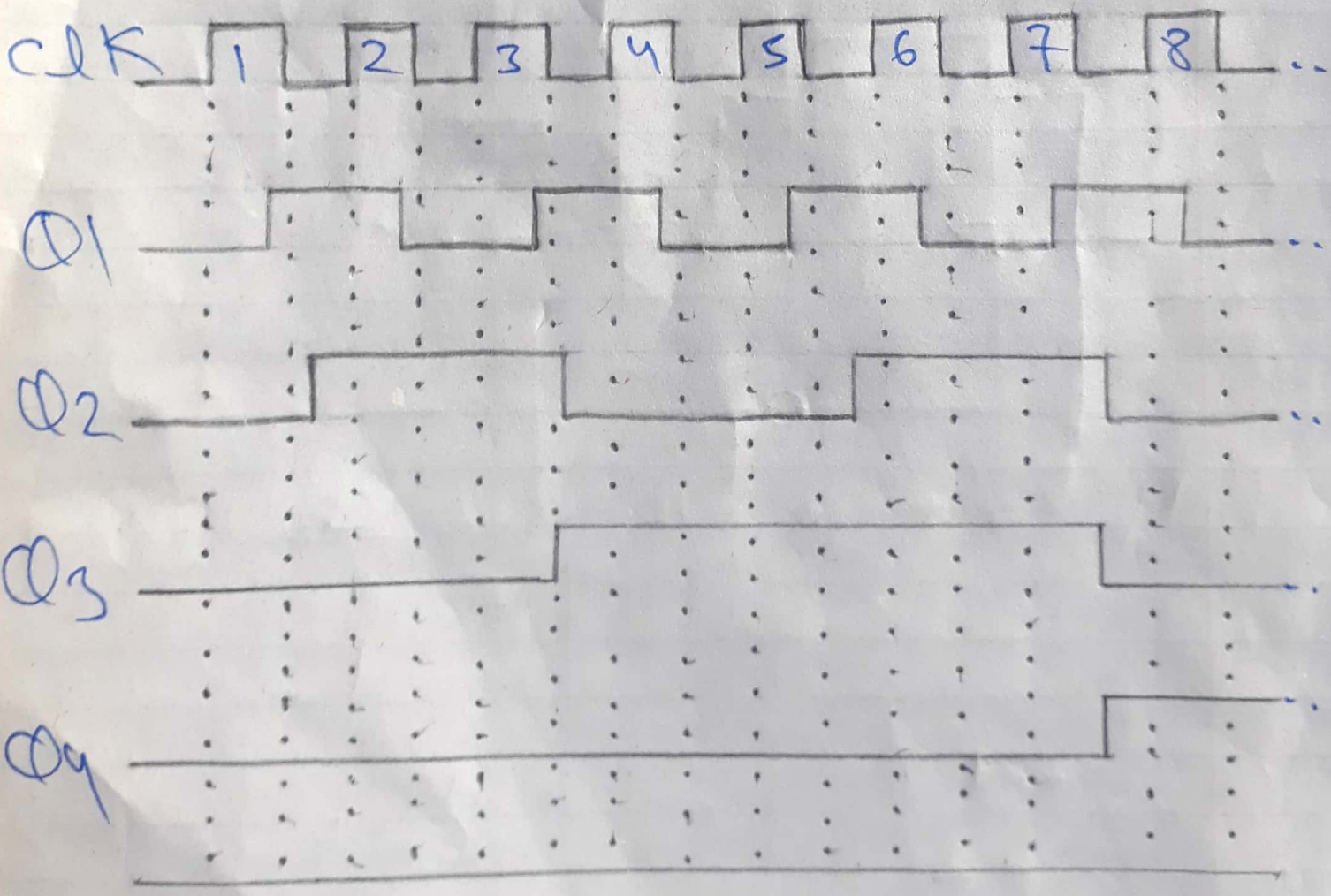
The registers are initially cleared.

(6)

Q6) Draw the logic Diagrams and timing diagram

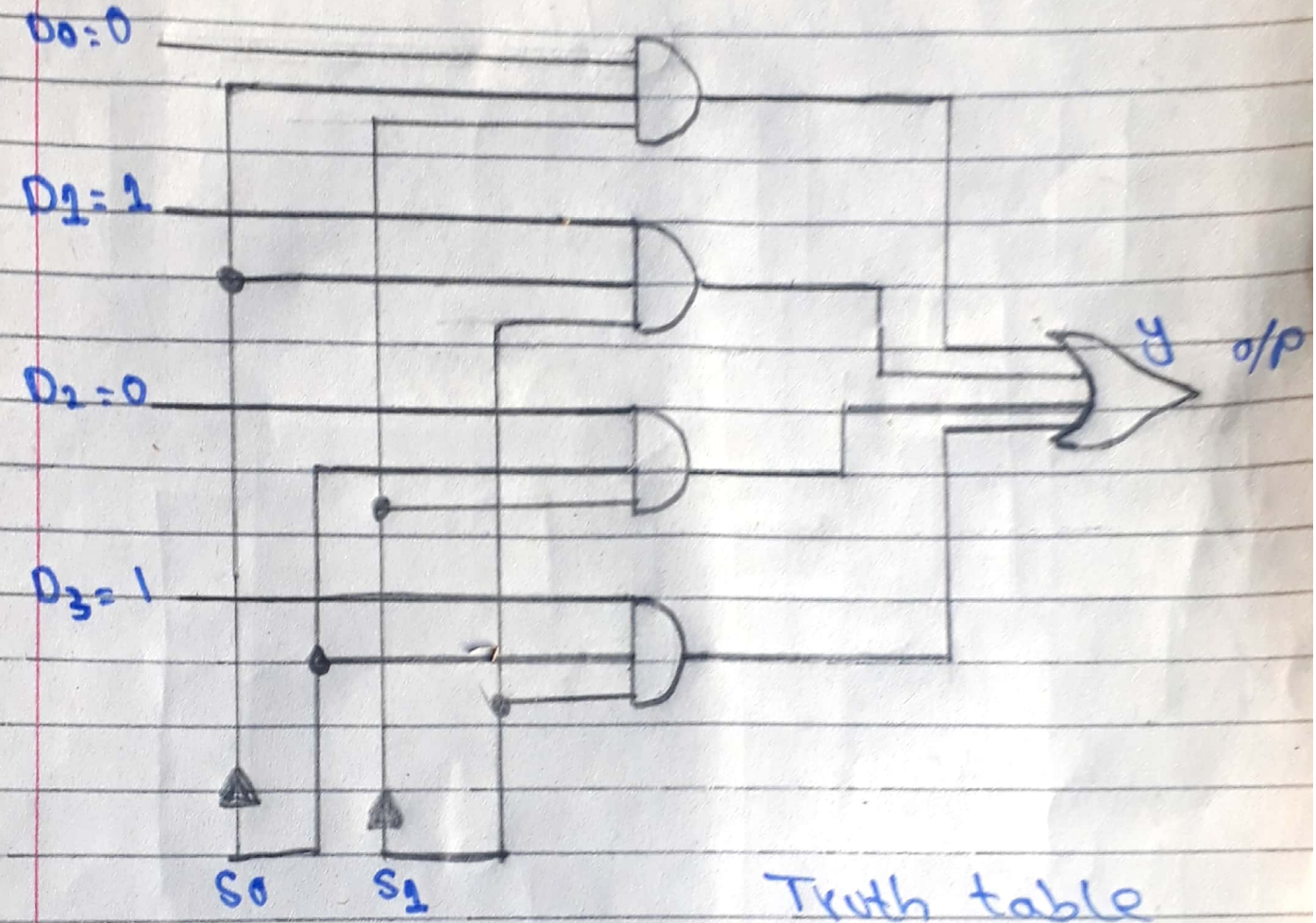
Ans)





Q2)

Circuit diagram



Truth table

S_1	S_2	I/p
0	0	$D_0 = S_0 S_1$
0	1	$D_1 = S_0 S_1$
1	0	$D_2 = S_0 S_1$
1	1	$D_3 = S_0 S_1$

Q2

(a) $S_0 = 1$, $S_1 = 0$

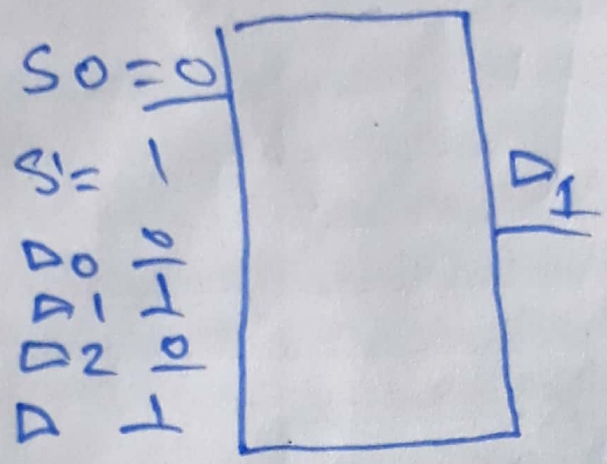
S_0	S_1	y
1	0	0

Q2

(b) $S_0 = 0$, $S_1 = 1$

S_0	S_1	y
0	1	1

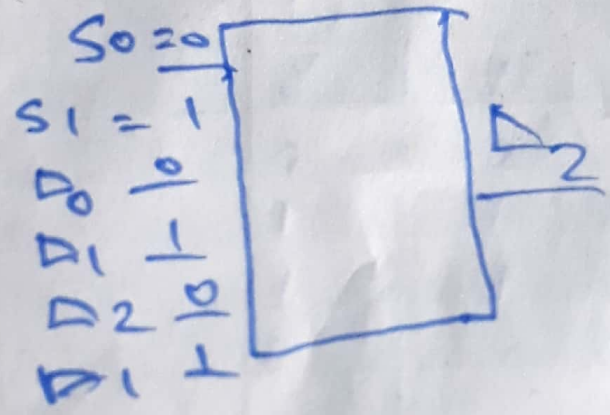
(02) b) $S_0 = 0$, $S_1 = 1$



$S_0 . S_1$ D_1

0 . 1

(02) c) $S_0 = 1$, $S_1 = 1$

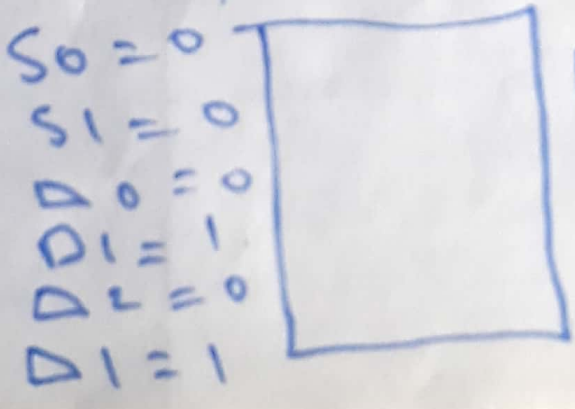


$S_0 . S_1 = D_2$

1 . 0

~~$S_0 . S_1 = D_1$~~

(02) d) $S_0 = 0$, $S_1 = 0$



y

$S_0 . S_1 = D_3$

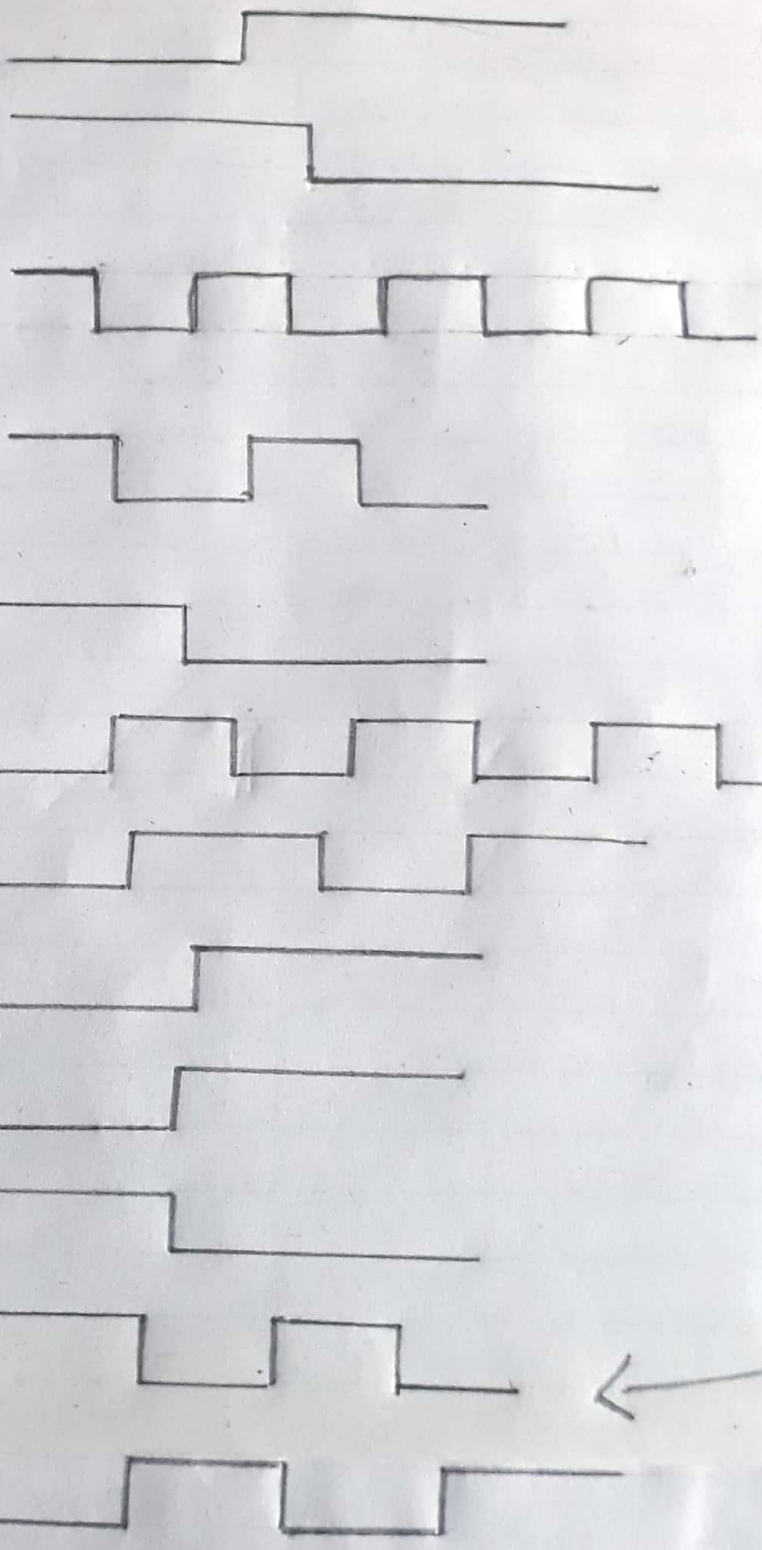
1 . 1

Q3

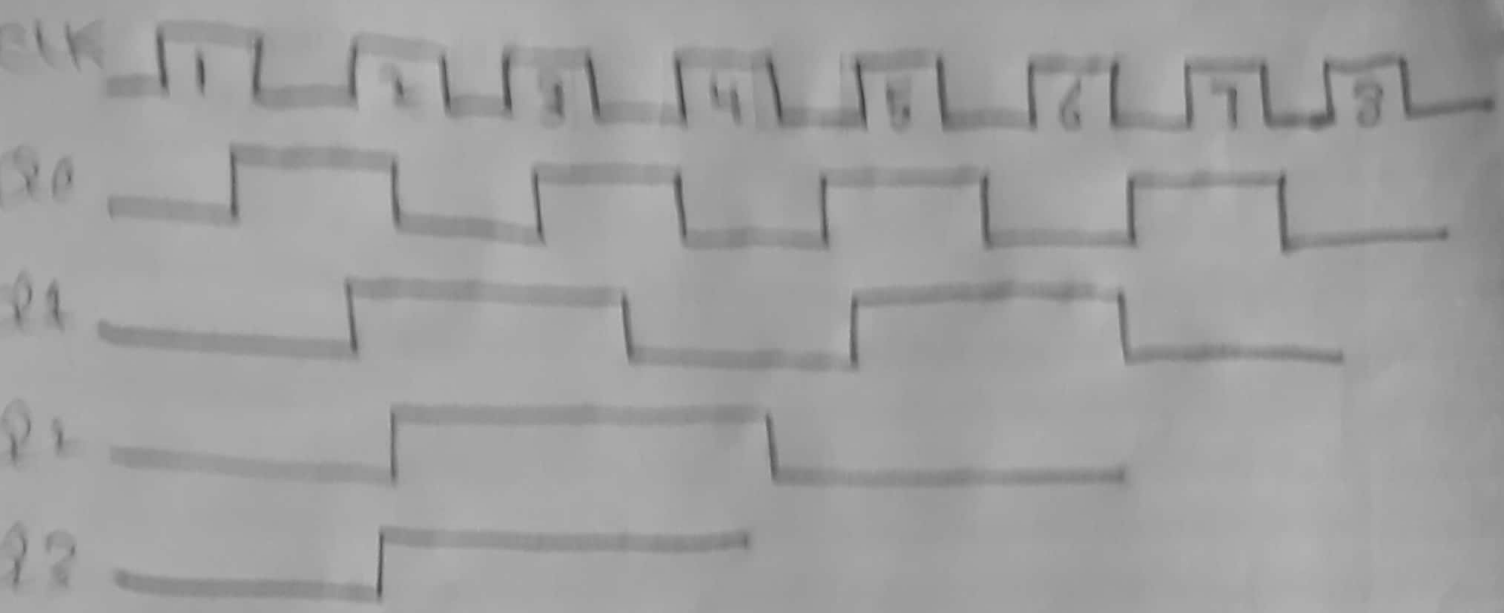
Ans 3).

3 even

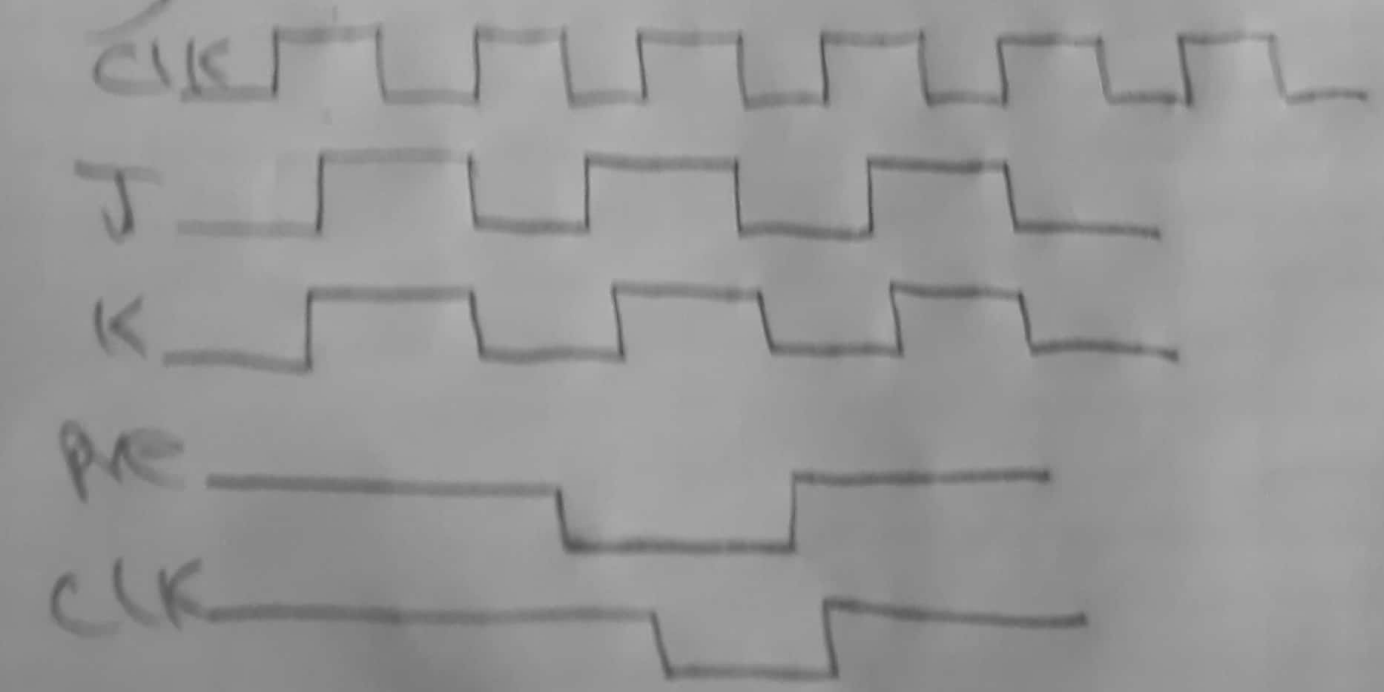
odd.



(10)



Ans)



End of Paper