NAME: AMIT SINGH

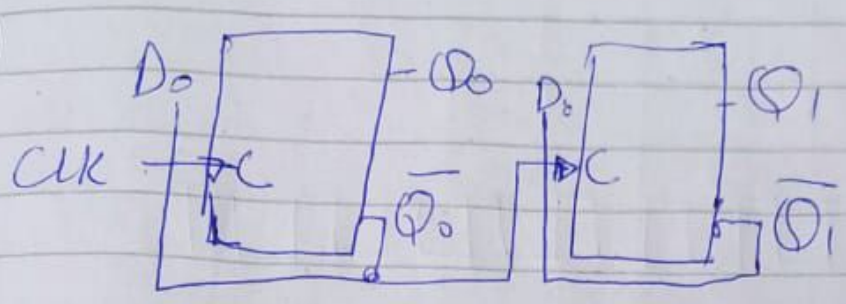
ID: 15478

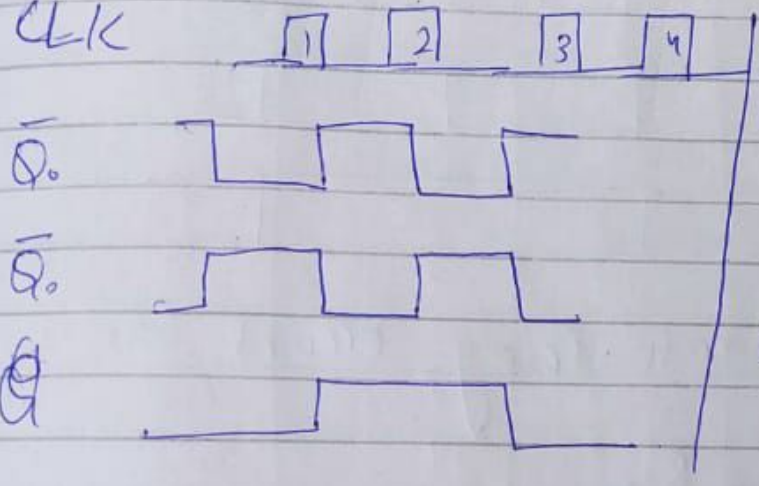
SUBJECT: DIGITAL LOGIC DESIGN

SEMESTER: 3RD

PROGRAMME: BS (SOFTWARE ENGINEERING)

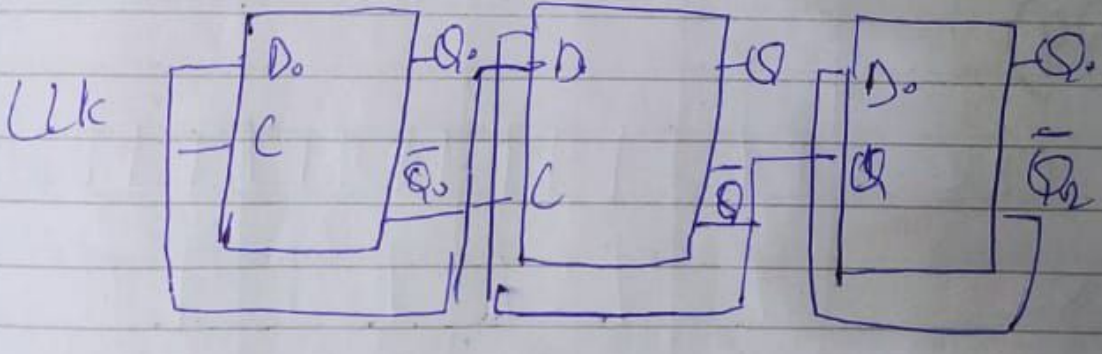
Q1)

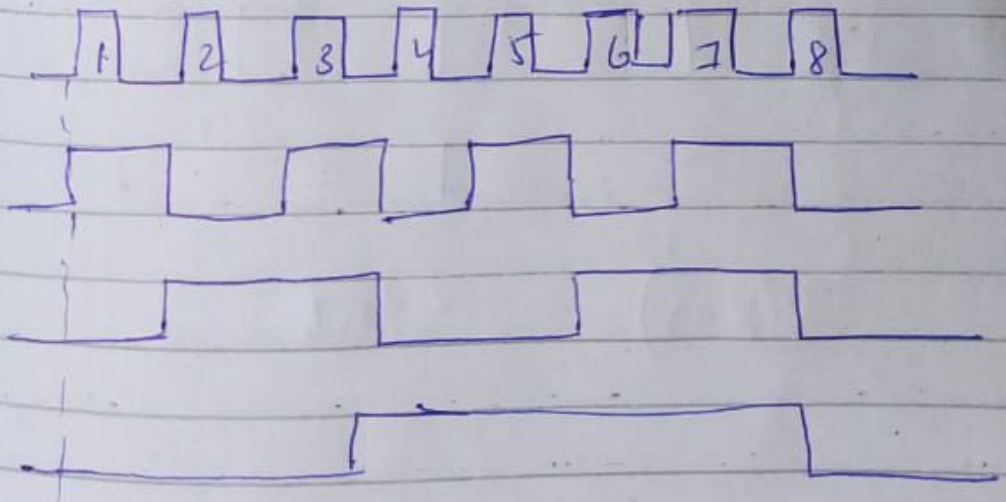




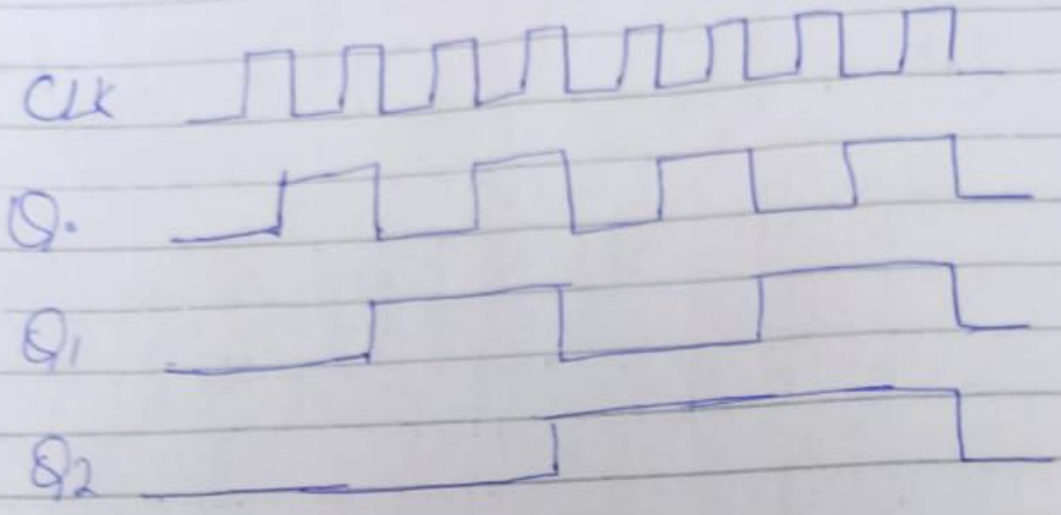
Checkpoint	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4	0	0

Q2





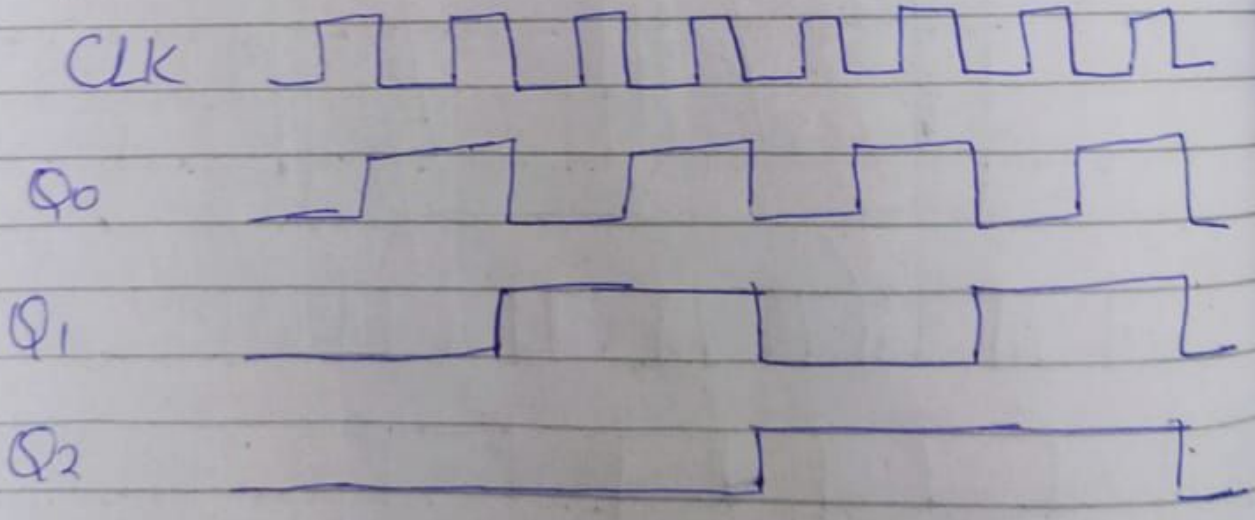
Q3)



The worst case delay occurs on

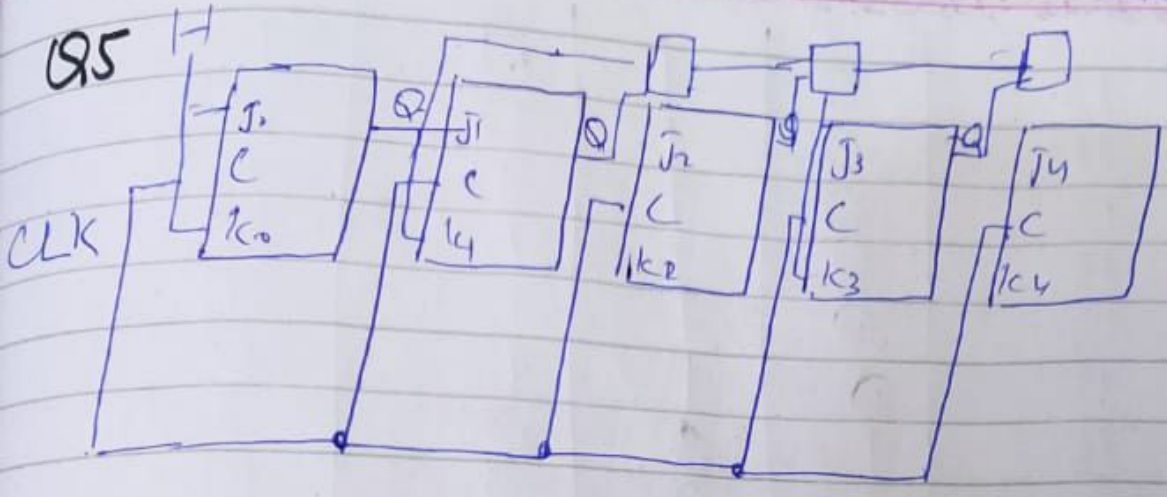
Clk - Q0

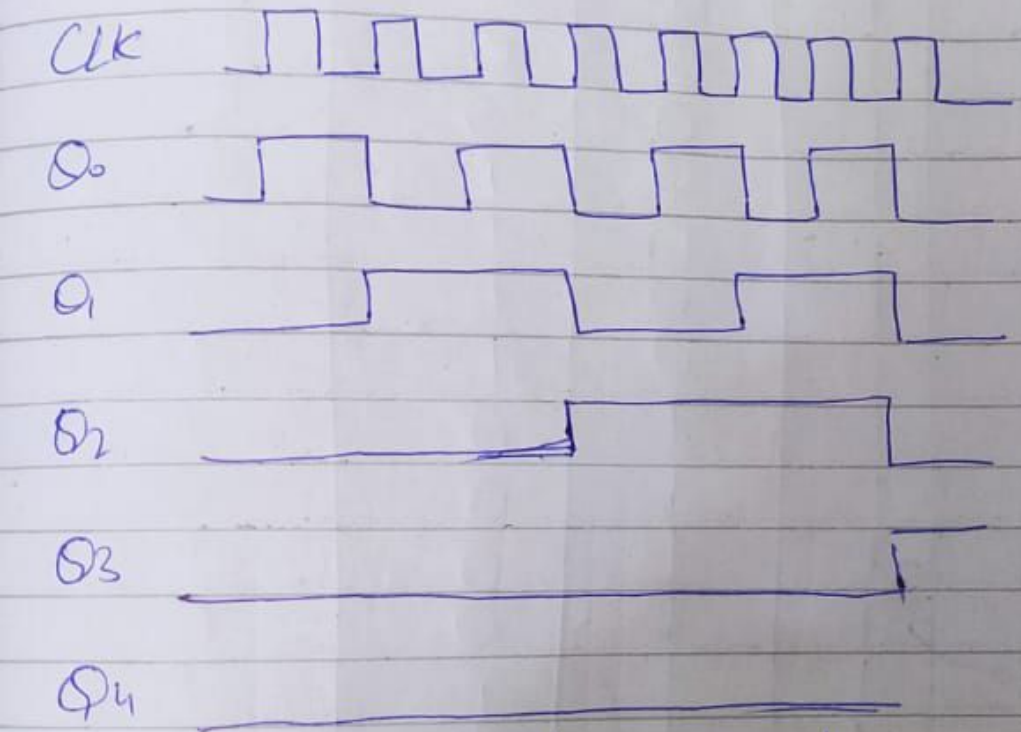
Q4)



3(8 ns) = 24 ns

Q5





C Pulse	Initially	Q_0	Q_1	Q_2	Q_3	Q_4
		0	0	0	0	0
1		0	0	0	1	1
2		0	0	0	1	0
3		0	0	1	0	1
4		0	0	1	0	0
5		0	0	1	1	1
6		0	0	1	1	0
7		0	1	0	0	1
8		0	1	0	0	0
9						

0	0	1	0	1
10	0	1	0	0
11	0	1	1	1
12	0	1	1	0
13	0	1	1	1
14	0	1	1	0
15	0	1	0	0
16	1	0	0	0
17	1	0	0	1
18	1	0	0	0
19	1	0	0	1
20	1	0	1	0
21	1	0	1	1
22	1	0	1	0
23	1	0	1	1
24	1	1	0	0
25	1	1	0	1
26	1	1	0	0
27	1	1	0	1
28	1	1	1	0
29	1	1	1	1
30	1	1	1	0
31	1	1	1	1