Assignment#3

Name Ikramullah
ID# 15072
Department BS(CS)

Ans#1

The first is to disable interrupts while an iterrupts is being processed A disabled interrupt simply means that the processor can and will ignore that interrupt request signal.

Ans#2

A second approach is to defined properties for interrupts and to allow an interrupt of higher priority to cause a lower-prioprity interrupt handler to be itself interrupted

Ans#3

Memory to processor

The processor reads an instruction or a unit of data from memory

Processor to memory

The processor write a unit of data to memory.

I/o to processor.

The processor reads data from an I/o devices via an I/o module

Processor to I/O:

The processor sends data to the I/O devices.

I/O to or from memory

For these two case, an I/O module is allowed to exchange data directly with memory, without going through the processor using direct memory access.

Ans#4

QPI Protocol layer

In this layer, the packet is defined as the unit of transfer. one key function performed at this level is a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent. A typical data packet payload is a block of data being sent to or from a cache

Ans#5

Physical and logical Architecture of Pcie.

A root Complex device also referred to as a chipset Connect the processor and memory system to the PCI express switch fabric Compisising

Ans#6

instruction cycle

The processing required for a single instruction is called an instruction cycle.

Ans#7

instruction cycle state diagram

instruction address calculation

Determine the address of the next instruction to be executed, usually this involves adding a fixed number

From its memory location into processor

instruction Fetch.

Read instruction from its memory location into the processor.

instruction operation decoding.

Analyze instruction to determine type of operation to be performed and operand to be used.

operand address Calculation.

if the operation involves reference to a operand in memory or available via I/O.

operand Fetch.

Fetch the operand from memory.

Data operation

performed the operation indicated inthe instruction.

Operand store

write the result into memory or out to I/O

Ans#8

Programing in Hardware.

Suppose we construct a general purpose configuration of ALU function This set of hardware will perform various functions on data depending on controll signals applied to the hardware. in the original case of customized hardware.

Programing in Software.

The new method of programing which is sequence of code is called software program

Ans#9

In the interrupt cycle the processor checks to see if any interrupts have occurred indicated by the presence of an interrupt signal.

Ans#10.

A disable interrupt simply means that the processor can and will ignore that interrupt request signal.

Ans#11.

Memory : 300 : 3005 ; 301, 5940 ; 302 ; 7006
Step1: 3005 → IR ; Step 2 : 3 → AC Step 3
5940 → IR Step4 : 3 + 2 = 5 → AC Step : 7006
→ IR ; step6. AC → Device 6

Ans#12

Clock style =
1 = 125 ns 8MHZ Bus cycle = 4 x 125 ns =
500 ns bytes transferred every 500 ns
thus transfer rate 4 MBytes/Sec
Doubling the frequency may mean adopting a new chip manufetusing technology. Doubling the external data bus means wider case. the speed of the memory chips will also need to double not to show down the microprosessor inthe second case the wordlength of the memory will have to double to be able to send / receive 32-bit quantities.

Ans#13

During a single bus cycle the 8-bit microprocessor transfer one byte while the 16-bit microprocessor transfer two bytes. The 16-bit microprocessor has twice the data transfer rate suppose we do 100 transfer of operand and instruction of which 50 are one byte long and 50 are two bytes long. The 8 bit microprocessor takes 50+(2x-16-50)=150 bus cycle for the transfer. The 16 bit mp requires 50+50=100 bus cycle. Thus the data transfer rates differ by a factor 1.5.

Ans#14

A Bus cycle takes 0.25 μs 0.25 so a memory cycle takes μs. if both operands are even aligned it takes 2 μs to fetch the two operation if one is odd-aligned the time required is 3 μs. if both are odd-aligned the time required.