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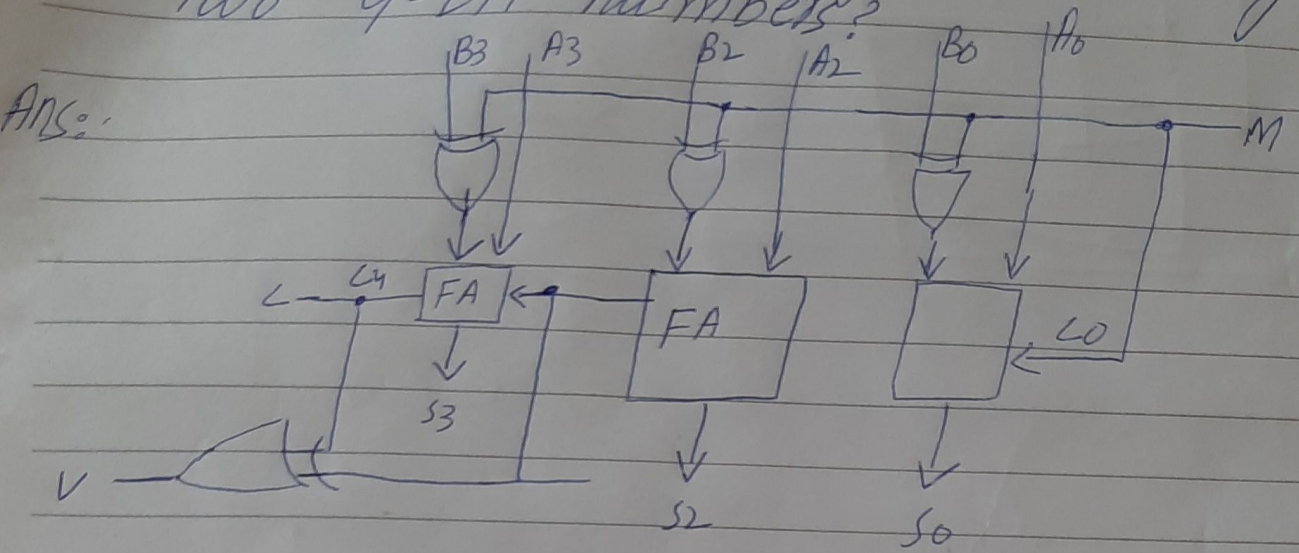
major Assignment for final term - Summer -

Subject Digital logic Design.

Q1:: Draw and Explain the logic diagram for each of the following

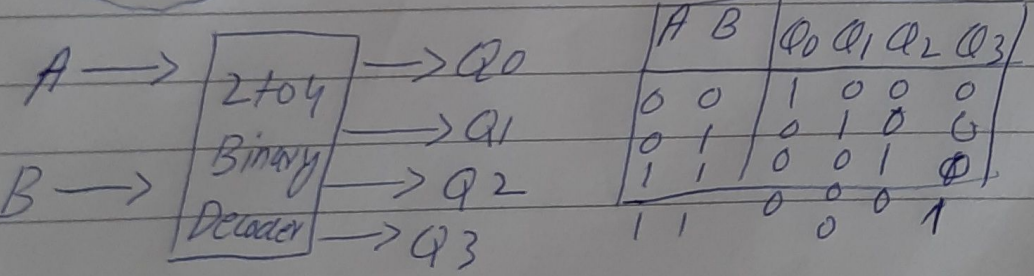
A:: A circuit for adding or subtracting two 4-bit numbers?

Ans::



For subtraction M=1. 1 is chosen because m act as the carry-in Therefore, all bits of B will be inverted and 1 will be added to the LSB to Find the 2's complements For addition, m=0 Therefore, carry-in set to zero as desired.

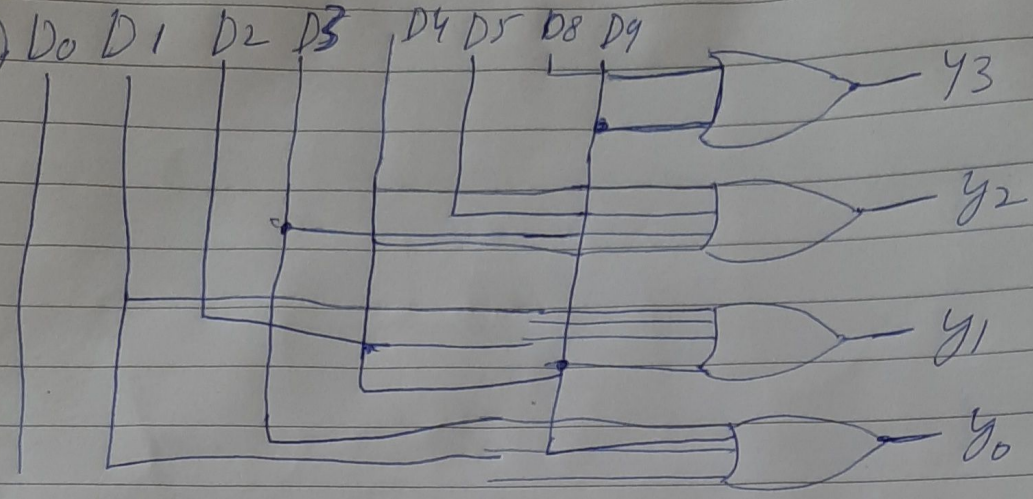
(B) 4 bit active low decoder::



A	B	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	1	0	0	1	Ø
1	1	0	0	0	1

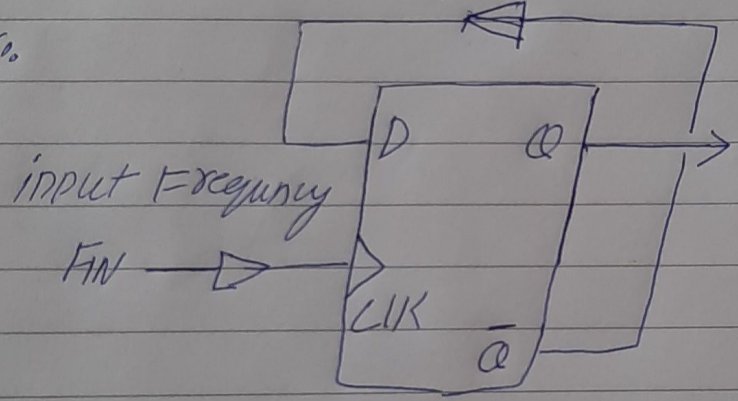
(c) Decimal to BCD encoder:-

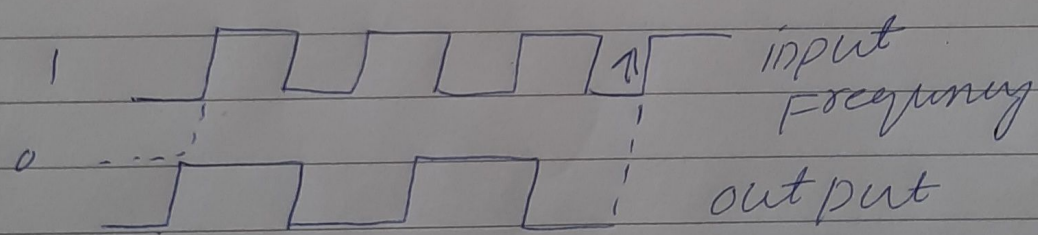
Ans:-



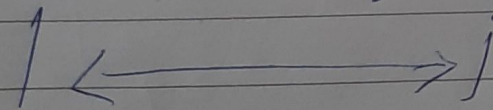
(d) Frequency divider (use 3-J-K Flip-Flops and assume 16 KHz Frequency of the initial wave-form?

Answer:-





Frequency = $\frac{f}{2}$



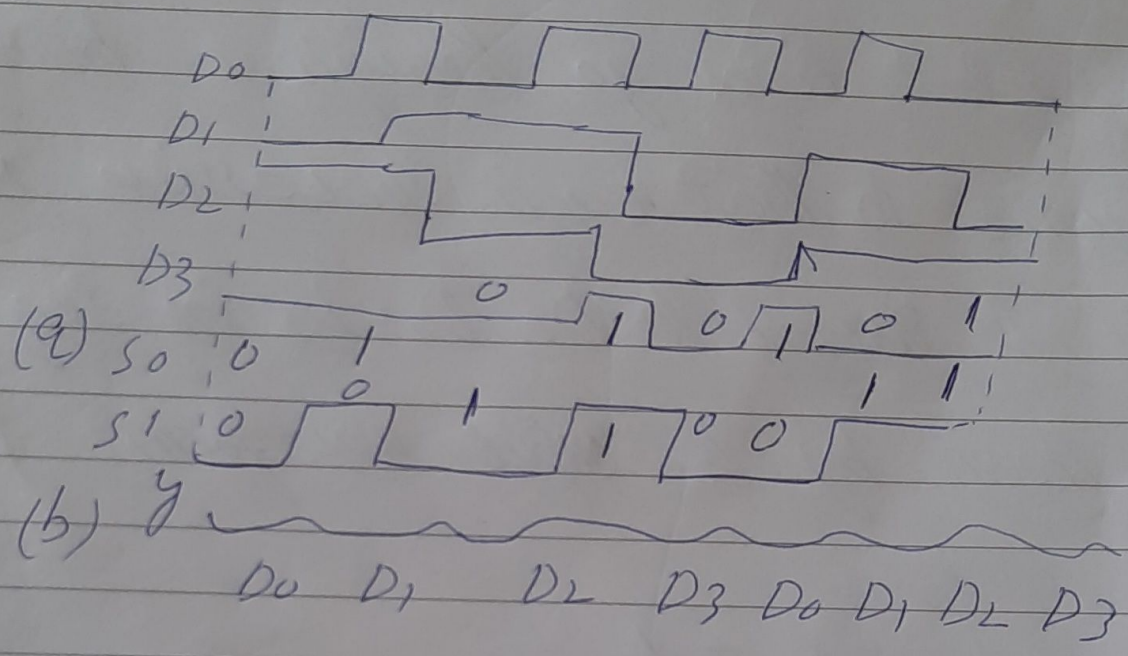
Q2: For the 4bit-input multiplexer, data input are given as:

$D_0 = 0,\ D_1 = 1,\ D_2 = 0,\ D_3 = 1$

Find the output y if the select inputs are given as:

(a) $S_0 = 1,\ S_1 = 0$

Ans:

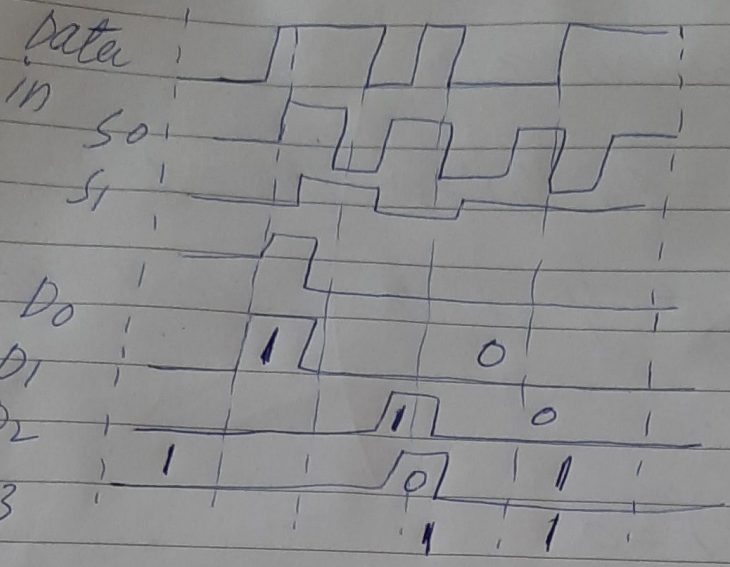


The binary state of the data select input during each interval determines which data input is selected. Notice that the data selected.

(4)

(b) $S_0 = 0$, $S_1 = 1$

Ans

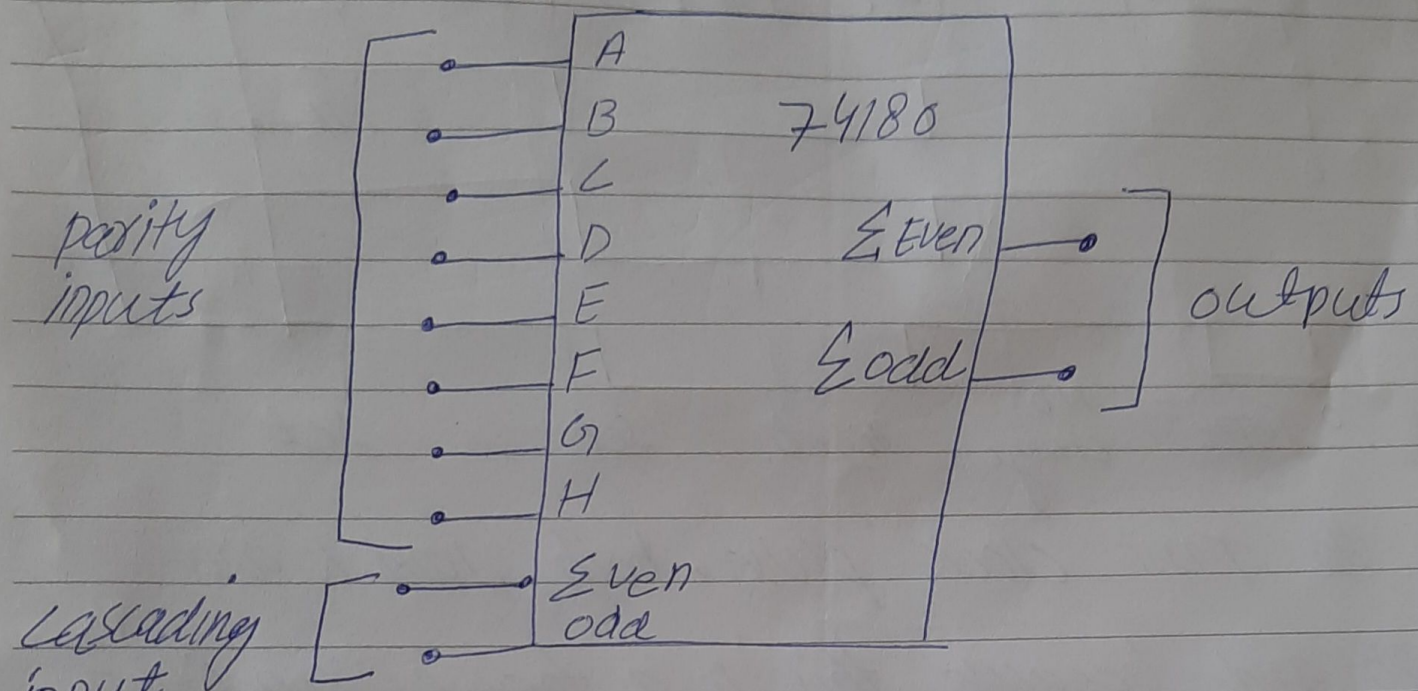


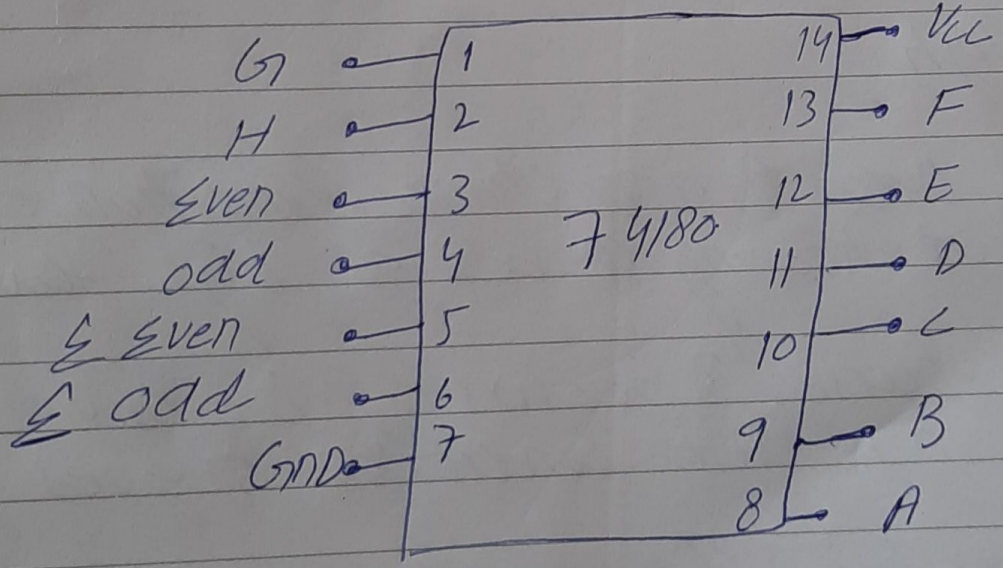
. The select lines go through a binary sequence so that each successive input bit is routed to D_0, D_1, D_2 in sequence as shown by the output waveform.

(c) $S_0 = 1$, $S_1 = 1$

Ans:

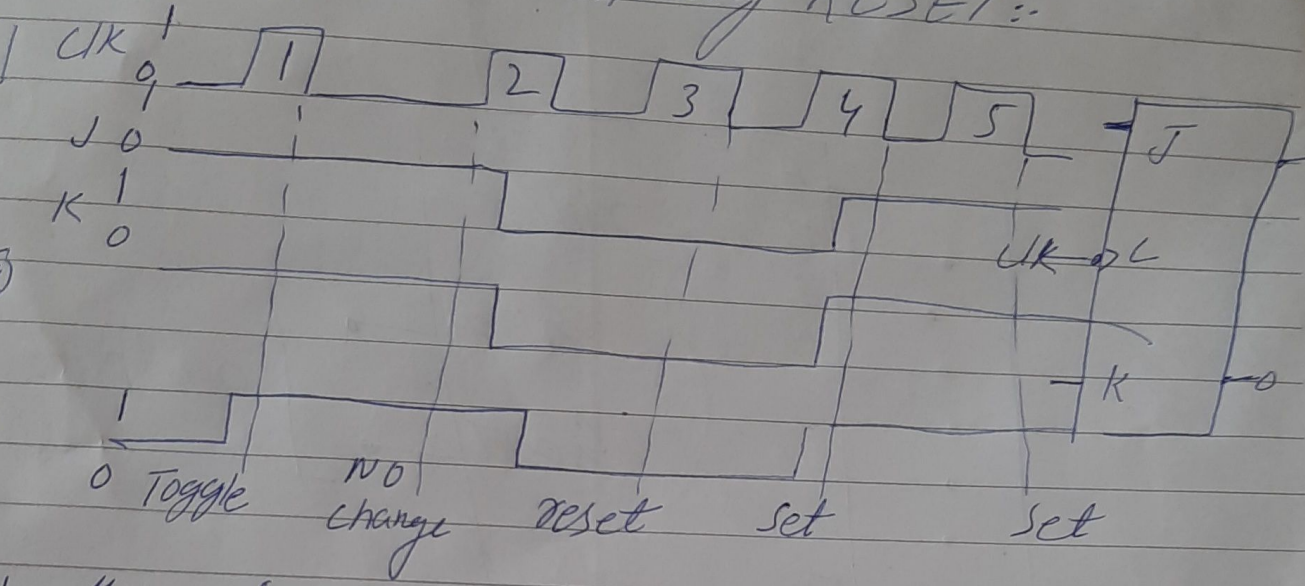
(3) Timing diagram in figure 01 shows inputs to a 9bit parity checker. Draw the Σ Even and Σ odd output for the even parity checking..





Q4: The waveforms in figure 02 are applied to the J, K clk, $\overline{PRE}$ and $\overline{CLR}$ inputs as indicated. Determine the Q output if the Flip-Flop is initially RESET:

Ans



(1) At the First clock pulse, both J and K are high and because this is a toggle condition Q goes high

(2) At clock pulse 2, a no change condition exists on the inputs, keeping Q at a high level

(3) When clock pulse 3 occurs J is low resulting in a set condition Q goes high

(4) A set condition still exists on J and and K when clock pluse 5 occurs so Q will remain high.

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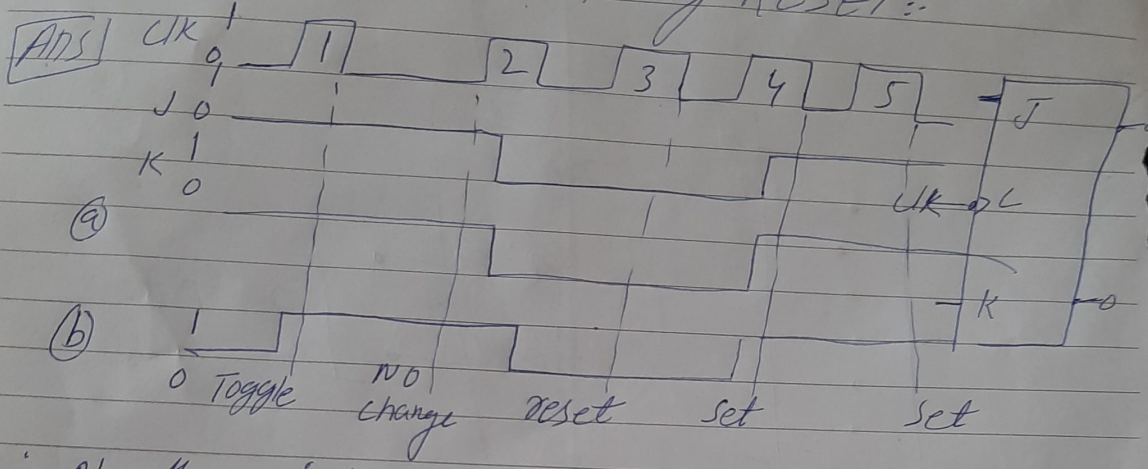
Ans:



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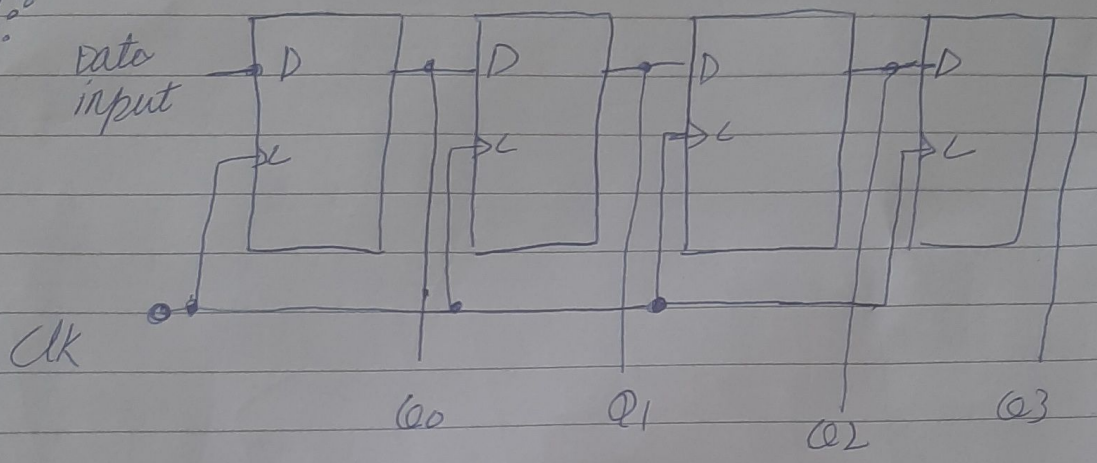
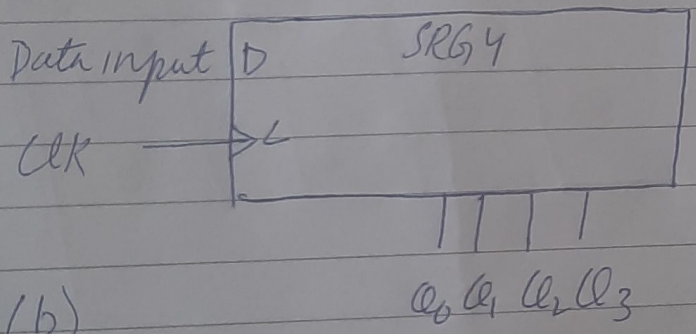
(7)

Q5:: Use the the waveforms in a Figure 03 to draw the timing digram For the parallel outputs (Q_1, Q_2, Q_3, Q_4) For the shift register Assume that register is initially cleared.

Answer::





(b)

Q6:-

Draw the logic ~~diagic~~ diagram and timing diagram for the 4-stage synchronous binary counter. Varify that the waveforms of the Q outputs represent the proper binary number after each clock pulse:-

Answer:-