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Program: B-Tech (CE)

Subject: VLSI

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Assignment

Q1 => Consider a resistive load inverter circuit with

$V_{DD} = 5V$, $K_n = 20\mu A/V^2$, $V_{TO} = 0.8V$

$R_L = 200K$ (ohm) $W/L = 2$

Calculate the critical voltage V_{OL}, V_{OH}, V_{IL}, V_{IH} on the VTC and Find the noise margins of the CKT?

Solution -

(i) => $V_{OH} = V_{DD}$

$$\boxed{V_{OH} = 5V}$$

=>(ii) $V_{OL} = V_{DD} - V_T + \frac{1}{K_n R_L} - \sqrt{\left(V_{DD} - V_T + \frac{1}{K_n R_L}\right)^2 - \frac{2V_{DD}}{K_n R_L}}$

$\Rightarrow$ But $k_n = k_n' \frac{W}{L}$

$= 20 \times 10^{-6} \times 2$

$k_n = 40 \times 10^{-6}$

$$V_{OL} = 5 - 0.8 + \frac{1}{40\times10^{-6}\times200\times10^{3}} - \sqrt{5-0.8+\frac{1}{40\times10^{-6}\times200\times10^{3}} - \frac{2\times5}{40\times10^{-6}\times200\times10^{3}}}$$

$V_{OL} = 4.325 - 2.174$

$\boxed{V_{OL} = 2.151\ V}$

(iii) $V_{IL} = V_T + \frac{1}{40\times10^{-6}\times200\times10^{3}}$

$V_{IL} = 0.925$

(4) $\Rightarrow V_{IH} = V_T + \sqrt{\frac{8}{3}\frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$

$= 0.8 + \sqrt{\frac{8}{3}\times\frac{5}{40\times10^{-6}\times200\times10^{3}} - \frac{1}{40\times10^{-6}\times200\times10^{3}}}$

$= 0.8 + 1.289 - 0.125$ $\rightarrow$

$$= \boxed{V_{IH} = 1.96V}$$

Now Noise margin

$$\Rightarrow N_L = V_{IL} - V_{OL}$$

$$= 0.925 - 2.15$$

$$\boxed{N_L = -1.225}$$

$$\Rightarrow N_H = V_{OH} - V_{IH}$$

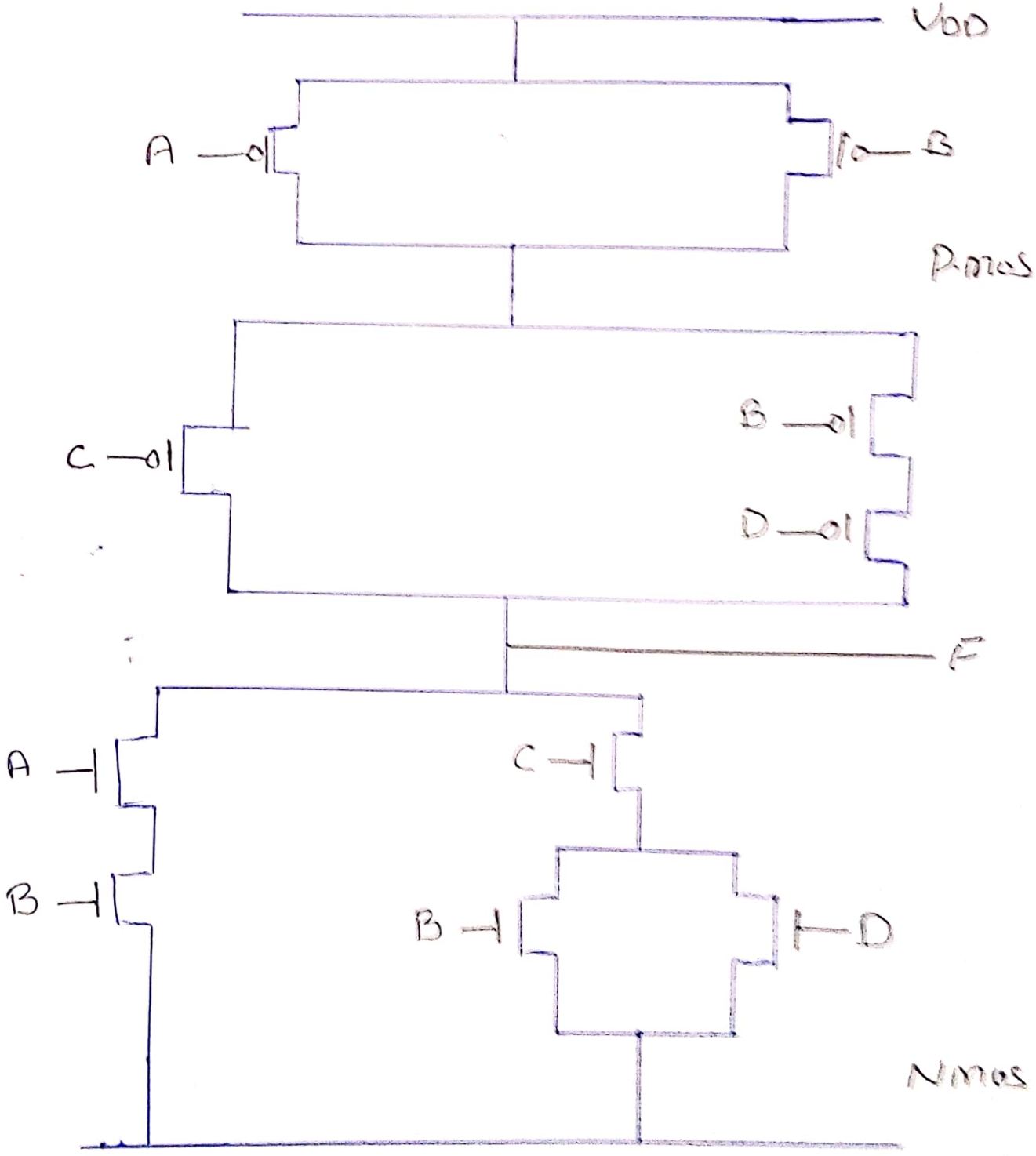
$$= 5 - 1.289$$

$$\boxed{N_H = 3.711}$$

Q2) Design a CMOS Logic Layout given the following Function.

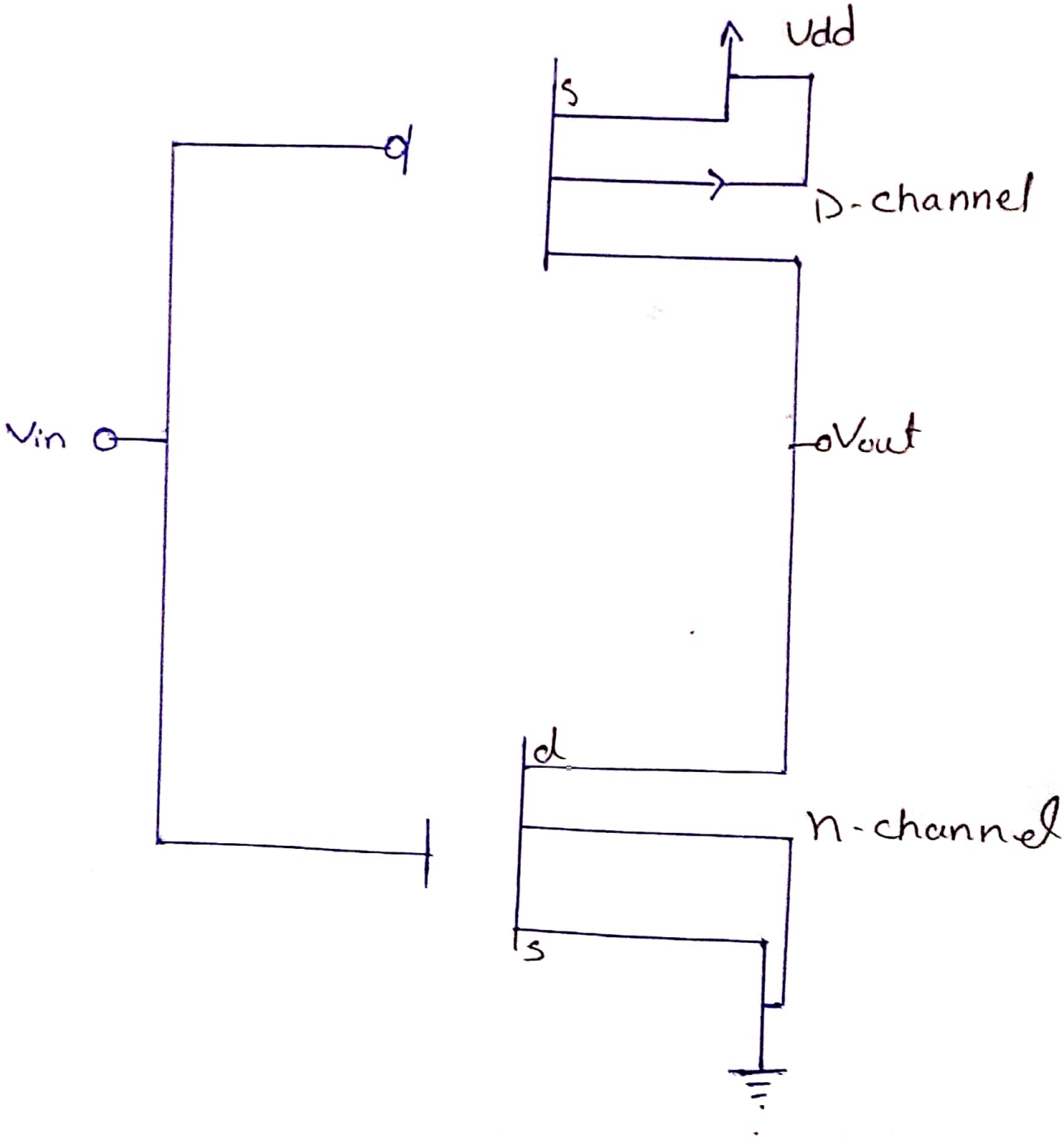
$$F = \overline{(AB + C)B + D}$$

Solution:-



Q(3) What is Mos inverter Also draw the CKT diagram of mos inverter.

Ans=>



This configuration is complementry mos.

=> Input connected to gate Terminal of Both the Transistor. That operated directly with input voltages. Substrate of the NMOS is connected To ground & substrate of pmos is connected To Power Supply VDD.

Q(4) write a note on depletion load NMOS inverter

Ans:- In integrated circuit depletion load NMOS is a form of digital logic family. that use for a single power supply voltage. earlier NMOS logic families that needed more than one different power supply voltage.

D.T.O.

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=> Although manufacturing these integrated circuits required additional processing steps, elimination of extra power supply and then improved switching speed, made this logic family the preffered choise for many microprossors and other logic elements. Some depletion load Nmos designs are still produced typically in parallel with newer CMOS counterparts.