IQRA NATIONAL UNIVERSITY

Name : Sauood Ur Rehman

Department : BS(CS)

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Submitted To :Muhammad Amin Sir

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Q1 Give answer to each of the following :

(A) . Discuss the two approaches for dealing with multiple interrupts

Ans The first is to disable interrupts while an interrupt is being processed. A disabled interrupt simply means that the processor can and will ignore that interrupt request signal.

The drawback to the preceding approach is that it does not take into account relative priority or time-critical needs.

2) A second approach is to define priorities for interrupts and to allow an interrupt of higher priority.

To cause a lower priority interrupt handler to be itself interrupted.

(B) Discuss the type of exchange that are needed by including the major forms of input and output for processor memory and I/O modules?

Ans: The type of exchange that are needed by indicating the major forms of input and output processor memory and I/O modules are.

Memory Processor: The processor read an instruction or a unit of data from memory
Processor to memory: The processor writes a unit of data to memory.

I/O To Processor: The processor read data from an I/O device via an I/O module.
Processor to I/O: To processor send data to the I/O device.
I/O to or from memory: For these two an I/O module is allowed to exchange data directly with memory without going through the processor using direct memory access.

(C) Discuss the Quick path interconnect (QPI) protocal layers?

Samuel Waldeman (B) 15031 (2)

Ans 9, QPI protocol layer or
In this layer, the packet is defined as the unit of transfer. One key function performed at this level in a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent. A typical data packet payload is a block of data being sent to or from a cache.

(1) Ans 10, Discuss physical and logical Architecture PCIe in detail.
Physical and logical Architecture of PCIe

* A root complex device also referred to as a chipset or a host bridge connect the processor and memory subsystem to the PCI Express switch fabric comprising one or more pcie and pcie switch device.
* Pcie links from the chipset may attach to the following kind of devices that implement PCIe.
* Switch : The switch manages multiple pcie streams.
* Pcie endpoint : An I/O device or controller that implement Pcie such as Gigabit ethernet switch a graphics or video controller disk interface or a communication controller.
* Legacy endpoint or legacy endpoint category in general for existing designs that have been migrated to PCI Express and it allows legacy behaviors such as use of I/O space and locked transaction.
* Pcie/PCI bridge : Allows older PCI devices to be connected to pcie-based systems.

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Q2 Write short note on each of the following?

(A) instruction cycle

Ans: The processing required for a single instruction is called instruction cycle. using the simplified two-step description given previously the instruction cycle is depicted. The two steps are referred to as the fetch cycle and execute cycle. Program execution halts only if the machine is turned off some sort of unrecoverable error occur or a program instruction that halts the computer is encountered.

(B) Instruction cycle and state diagram?

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Ans (d)

Instruction cycle state diagram.

The state in instruction cycle can be described as follows.

* Instruction address calculation (IAC): Determine the address of the next instruction to be executed. usually this involves adding a fixed number to the address of the previous instruction.

* Instruction fetch (IF): Read instruction from its memory location into the processor.

* Instruction operation decoding (IOD): Analyze instruction to determine type of operation to be performed and operand(s) to be used.

* Operand Fetch (OF): Fetch the operand from memory or read it in from I/O.

* Data operation (DO): Perform the operation indicated in the instruction.

* Operand Store (OS): Write the result into memory or out to I/O.

(e) classes of interrupts?

Ans (e)

Classes of interrupts:

I) Program: It is generated by some condition that occurs as a result of an instruction execution such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.

II) Timer: It is generated by a timer within the processor. This allow the operating system to perform certain function on a regular basis.

III) I/O: It is generated by I/O controller to signal normal completion of an operation, request service from the processor or to signal variety of error condition.

IV) Hardware failure: It is generated by failure such as power failure or memory parity error.

Saurav kr Parmar (6) 15031 (6)

(1)

Ans 8

Bus interconnection scheme

Bus interconnection scheme

The most common computer interconnection structures are based on the use of one or more system buses.

(a) Data lines :- The data lines provide a path for moving data among system modules. These lines collectively are called the data bus.

(b) Address lines :- The address line are used to designate the source or destination of the data on the data bus. The width of address bus determines the maximum possible memory capacity of the system.

(c) Control lines :- The control line are used to control the access to and use of data and address lines Because the data and address lines are shared by all components. Typical control lines include:
Memory write, Memory read, I/O write, I/O read Transfer-Ack, Bus request, Bus grant, interrupt request, interrupt Ack, clock and Reset.

(Q3) Differentiate each of the following:

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(A)

Ans 5.

Program flow of control without interrupt and with interrupt

Program flow of control without interrupt and with interrupt.

1) In the interrupt cycle the processor checks to see if any interrupt have occured indicated by the presence of an interrupt signals.

2) if no interrupt are pending the processor proceeds to the fetch and fetches the next instruction of the current program.

(B)

Disabled interrupt and nested interrupt Processing!

Ans 5

Disabled interrupt and nested interrupt

Disabled interrupt es simply mean that the processor can and will ignore that interrupt request signal.

nested interrupt es Is to allow an interrupt of higher priority to cause a lower priority interrupt handler to be it self interrupted.

(C)

Ans 5

Programing Hardware and Programing Software

Programing in Hardware es suppose we construct a general purpose configuration of arithmatic and logic function. This set of Hardware will perform various function on data in the original case of customized Hardware the system accept data and produced result.

Programming in Software of

The new method programming is much easier instead of rewriting the hardware for each new program. All we need to do is provide a new sequence of code. Each code is in effect an instruction and part of the hardware interprets each instruction and generates control signal.

Q4 Solve each of the following?

(A) The hypothetical machine of has two I/O instruction.

0011 = load AC from I/O
0111 = store AC to I/O

in these cases the 12 bit address identifies a particular I/O device show the program execution (using the format identifies particular I/O device. Show the program execution using the figure 3.5) for the following program

load AC from device 5
Add content of memory 940
store AC to dive 6.

Assume that the next value retrieved from device 5 is 3 and that location 940

9) Ans (A) (C)

Memory (content in hex) 300: 3005;
301: 5940; 302: 7006 step 1: 300 → IR; step 2: 3 → Ac step 3:
5940 → IR; step 4: 3+2 = 5 → Ac
step 5: 7006 → IR; step 6: Ac → Device 6

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(B)

Ans (C) B,

"The program execution" of figure 02 is described in the text using six steps.
Six steps are

1) (a) The PC contains 300 the address of the first instruction. This value is loaded into the MAR.
(b) The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR.

and the PC is interconnected. These two steps can be done in parallel.

(c) The value in the MBR is loaded into the IR.

2) (a) The address position of the IR (940) is loaded into the MAR.

(b) The value in location 940 is loaded into the MBR.

(c) The value in the MBR is loaded into the AC.

3) (a) The value in the PC (301) is loaded into the MAR.

(b) The value in location 301 (which is the instruction and the value (5941)) is loaded into the MBR and the PC is incremented.

(c) The value in the MBR is loaded into the IR.

4) (a) The address position of the IR (941) is loaded into the MAR (b) value in location 941 is loaded into the MBR.

(c) The value of location MBR are added and the result is stored in the AC.

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5) (a) The value in the PC (302) is loaded into the MAR.
(b) The value in location 302 (which is the instruction with the value 2941) is loaded into the MBR, and the PC is incremented.
(c) The value in the MBR is loaded into the IR.

6) (a) The address portion of the IR (941) is loaded into the MAR.
(b) The value in the AC is loaded the MBR
(c) The value in the MBR is stored in location 941.

Ans 5 (C)

How many bits are needed for the program counter and the instruction register?

(a) $2^{24} = 16$ MBytes and the instruction register?

(b) (1) if the local address bus is 32 bit the whole address can be transferred at once and decoded in memory. However because the data bus is only 16 bits, it will require 2 cycles to fetch a 32 bit instruction or operand.

(2) The 16 bits of the address placed on the address bus can't access the whole memory interface control is needed to catch and first parts of the address and then the second part.

(c) The program counter must be at least 24 bits. Typically a 32-bit microprocessor will have a 32 bit external address bus and a 32 bit program counter, unless onchip segment register are used that may work with a smaller program counter if the instruction register is to contain the whole instruction, it will have to be 32-bit long if it will contain only the op code (called the op code register) then it will have to be 8bits long.

(D) consider two microprocessor having 8 and 16 bit-wide external data buses. respectively The two processor are identical otherwise and their bus cycle take just as long.

(a) suppose an instruction and operands are two bytes long. By what factor do the maximum data transfer rates differ ?

(b) ~~suppose~~ Repeat if half of the operand and instruction are one-byte long.

Ans 3 ~~Ans~~ (a) During a single bus cycle the 8 bit microprocessor fetched one byte. while the 16 bit microprocessor

has twice the data transfer rate.

b) Suppose we do 100 transfer of operands and instruction of which 50 are one byte long and 50 are two bytes long. The 8 bit microprocessor takes 50+(2×16-50)=150 bus cycles for the transfer. The 16 bit microprocessor required 50+50=100 bus cycles. Thus the data transfer rates differ by a factor of 1.5.

(c) The intel 8086 is a 16 bit processor similar in many ways to the 8 bit 8088. The 8086 uses a 16 bit bus that can transfer 2 bytes at a time provided that then lower-order byte has an even address. However the 8086 allows both even- and odd-aligned word operands. If an odd aligned word is referenced two memory cycles, each consisting of four bus cycles are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it take to fetch the operand. Give the range of possible answers. Assume a clocking rate of 4 MHz and no wait states.

Ans: A bus cycles takes 0.25 μs. So a memory cycle take 1 μs. if both operands are even aligned it take 2 μs to fetch the two operand if one is odd-aligned the time acquired is 3 μs. if both are odd aligned the time required is 4 μs.

(E) Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that an average 20% of the operands and instruction are 32 bits long 40% are 16 bit and 40% are only 8 bit long. Calculate the improvement achieved when fetching instruction and operand with the 32-bit microprocessor.

Ans: Consider a mix of 100 instruction and operands on average they consist of 20% 32 bit items. 40% 16 bit items and 40% 8 bit items. The number of bus cycles required for the 16 bit microprocessor is (2×20)+40+100 = 120. For the 32 bit microprocessor the number required is 100. This amount to an improvement of 20/120 or about 17%.