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Assignment 1<sup>st</sup> (Chap 1)

Q) What are four main functions of a Computer.

Ans **Data processing:-**

Data may take a wide variety of forms & the range of processing requirements is broad.

**Data storage:-**

The computer perform a long term data storage function. file of data is stored.

**Data movement:-**

When data is moved over longer distances, to or from is called data communication.

**Control:-**

Within the computer, a control unit manages the computer's resources the performance of its functional parts in response to instructions.

B. Figure 01 shows the IBM Z Enterprise EC12 CoE layout briefly. Explain the function of each area.

### ISU (Instruction Sequence unit):-

Determines the sequences in which instructions are executed in what is referred to as superscalar architecture.

### IFU (Instruction fetch unit):-

Logic for fetching instruction.

### IDU (Instruction decode unit):-

IS responsible for parsing & decoding of all Z/architecture operation code.

### LSU (Load-store unit):-

It is responsible for handling all types of operand access of all lengths in the Z/architecture.

### XU (transmission unit):-

This unit translates logical addresses from instruction into physical addresses in the main memory. It contains TLB used to speed memory access.

### FXU (fixed point unit):-

The FXU executes fixed-point arithmetic operations.

### BFU (binary floating unit):-

The BFU handles all binary & hexadecimal floating operations as well as fixed point multiplication operation.

## DFU (decimal floating point unit) :-

The DFU handles both fixed point & floating point operation on numbers that are stored as decimal digits.

## RU (recovery unit) :-

The RU keep a copy of the complete state of the system.

## Cop (dedicated co-processor) :-

The Cop is responsible for data compression & encryption function for each core.

## L1 - Cache :-

There is a 64-kb L1 instruction code cache allowing the ipu to prefetch instruction before they are needed.

## L2 - Control :-

This is the control logic that manages the traffic through the two L2 cache.

## Data L2 :-

A 1-MB L2 data cache for all memory traffic other than instructions.

## Instr - L2 :-

A 1-MB L2 instruction cache

C. Discuss the IAS operation using the flowchart in Fig 02.

Ans The IAS operates by respectively performing an instruction cycle. Each instruction consists of two sub-cycle.

Fetch cycle:

The opcode of next instruction is loaded into the IR & the address portion is loaded into the MAR. This instruction may be taken from the IBR; or it can be obtained from memory by loading a word into MBR, & then down to the IBR IR & MAR.

Executive Cycle:

The control circuitry interprets the opcode & execute the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by ALU.

D. For each of the following examples, determine whether this is an embedded system explaining why or why not.

a. Are programs that understand physics &/or hardware embedded? e.g. one that uses finite-element methods to predict fluid flow over airplane wings.

Ans) No, these programs are never considered to be embedded because they are not an integral component of a larger system.

b) Is the internal microprocessor controlling a disc drive an example of an embedded system.

Ans Yes, regardless of what the disc drive is used for. The software (firmware actually) within the disc drive controls the HDA hardware & is hard real time as well.

c. I/O drivers control hardware, so does the presence of an I/O driver simply that the computer executing the driver is embedded?

Ans. No I/O drivers do not represent the embedded system.

d. Is the microprocessor controlling the cell phone an embedded system?

Ans) Yes the firmware in the cell phone is controlling the radio hardware.

e. Are the computer in a big phased array radar considered embedded? These radars are 10 story buildings with one to three 100-foot diameter radiating perches on the sloped sides of the buildings.

Ans Yes these computers were generally some of the most powerful computers available when the system was built, are located in large computer room occupying almost one whole floor of a building & may be hundreds of meter away from the radar hardware. However the software running in these computer control the radar hardware therefore the computer an integral component of a large system.

f. Is a PDA an embedded system?

Ans Yes, PDA is an embedded system because its just like a personal computer in hand.

g. Is a traditional flight management system (FMS) built into an airplane cockpit considered embedded?

Ans) If the FMS is not connected to the avionics & is used only for logistics computerization, a function readily performed on a laptop, then the FMS is clearly not embedded.

h. Are the computer in a hardware in the loop (HIL) simulator embedded?

Ans Yes, both in the simulator & in the thing being tested in the HIL simulator hardware is being controlled on both sides.

i) Is the computer controlling fuel injection in an automobile engine embedded?

Ans Yes, its a part of a large system, the engine & its directly monitoring & controlling the engine through special hardware.

j) Is the computer controlling a pacemaker in a person's chest an embedded computer?

Ans. Yes in this case of the system is the combination of the pacemaker & the person's heart.

Q Write note on the following.

A:- Main structural components of a computer:-  
There are four components of main structural:-

\*\* CPU:-

Control the operation of the computer & performs its data processing functions, often simply referred to as processor.

\* Main memory:-

Stores data.



\* I/O :-

Moves the data between the computers & its the external movement.

\* System interconnection:-

Some mechanisms that provides for communication among CPU, main memory & I/O.

b. Key characteristics of a planned computer family.

Ans Similar or identical instruction set:-

In some cases the lower end of the family has an instruction set that is a subset of that of the top end of the family. This means that program can move up but not down.

\* Similar or identical operating system:-

The same basic operating system is available for all family members.

\* Increasing Speed:-

The rate of instruction execution increases in going from lower to higher family members.

\* Increasing numbers I/O ports:-

The number of I/O ports increases in going from lower to higher family members.

\* Increasing memory size:-

The size of main memory increases in going from lower to higher family members.

## \* Increasing Cost:-

At a given point in a time the cost of a system increases in going from lower to higher family members.

## C) Stored Program Counter

Ans. A fundamental design approach first implemented in the IAS Computer is known as Stored Program Counter. This idea is usually attributed to the mathematician John von Neumann.

\* The first publication of the idea was in 1945 proposal by von Neuman for a new computer the EDVAC.

In 1946, von Neumann & his colleagues began the design of a new stored program computer, referred to as the IAS computer, it consists of

\* Main memory which stores both data & instructions.

\* An arithmetic & logic unit (ALU) capable of operating on binary data.

## D) Moore's Law:-

Moore's Law was propounded by Gordon Moore co-founder of Intel in 1965 (Moore's). Moore observed that the number of transistors that could be on a single chip was doubling every year.

The consequence of Moore's law are profound.

- 1) The cost of Computer logic & memory Circuitry has fallen at a dramatic rate.
- 2) Because logic & memory elements are placed closer together on more densely pack chips, the electric path length is shortened increasing operating speed.
- 3) There is a reduction in power requirements.
- 4) With more circuitry on each chip there are fewer interchip connections.

## Differentiate each of the following

A) Computer organization & Computer architecture

Ans Computer Organization:-

Refers to those attributes of a system visible to a programmer or put another way those attributes that have a direct impact on the logical execution of a program. A term that is often used interchangeably with Computer architecture is instruction set architecture.

Computer architecture:-

Refers to the operational unit & their interconnection that realize the architectural specification example of architectural attributes include the instruction set the number of

bits used to represent various data types (e.g. numbers, characters) I/O mechanism & techniques for addressing memory.

B) Microprocessor & Microcontroller:-

Ans) Microprocessor:-

Chips include registers an ALU & some sort of control unit or instruction processing logic. As transistors density increased it became possible to increase it ultimately to add memory & more than one processor.

Microcontroller:-

is a single chip that memory contains the processor, non-volatile memory for the program (ROM) volatile memory for input & output (RAM) a clock & an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessor & much higher energy efficiency.

C) RISC and CISC:-

The current X86 offerings represent the result of decades of design effort on complex instruction set computers (CISC). The X86 incorporates the sophisticated & serves as an excellent example of CISC design.

\* An alternative approach to processor design is reduced instruction set computer (RISC). The ARM architecture is used in a wide

Variety of embedded system & is one of the most powerful & best designed RISC based system on the market. In this section & the next - we provide a brief overview of these two system.

D) Cortex-A, Cortex-B, & Cortex-M

The Cortex A & Cortex-A50 are application processor intended for mobile devices such as smartphones & eBook readers, as well as consumer devices such as digital TV & home gateways (e.g. DSL & cable internet modems). These processor run at higher clock frequency (over 1 GHz) & support a memory management unit (MMU).

\* The Cortex-R is designed to support real time applications, in which the timing of events need to be controlled with rapid response to events. They can run at a fairly high clock frequency & have very low response latency.

\* Cortex-M Series processor have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt management is coupled with the desire for extremely low gate count & lowest possible power consumption.

Q4 Solve each of the following:

A. Given the memory contents of the IAS Computer show below,  
Address contents.

1. 08A010FA2/0FB
2. 08B010FA0F08D
3. 08C020FA2/0FB.

A. Show the assembly language code for the program, starting at address 08A.

Ans Here is a simple way to understand this problem.  
Contents are divided up into two 5 bit instruction LH & RH.

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since in this hexadecimal form you have to convert the number to binary form (use the IAS instruction set)

LH instruction :-

01 = 0000001 = Load M(x)

M(x) refer to the memory address location 0FA

The first 5 bits of 08A should read - load M(0FA) RH instruction.

21 = 00100001 = Store M(x)

Date: \_\_\_\_\_  
M(x) refer to the memory address location OFB.

The second 5 Bits of O8A should read  
STOR M(OFB)

Finally the assembly language code for  
O8A 010FA210FB is

LOAD M(OFA)

STOR M(OFB)

2. Here is a simple way to understand this  
problem.

Contents are divided up into two 5 Bits  
instruction LH & RH

LH instruction = 010FA

opcode = 01

address = OFA

RH instruction = 0F08D

opcode = 0F

address = 08D

Since this is in hexadecimal form you  
have to convert the number to binary form.

LH instruction:-

01 = 0000001 = Load M(x)

M(x) refers to the memory address location  
08D.

The first 5 bits of 08B should read - jump  
+M(08D, 0:19)

Finally the assembly language for 08B  
010FA0F08D is Load M(OFA)

jump +M(08D, 0:19)

3. Here is a simple way to understand this problem  
Contents are divided up into 5 bits instruction

LH & RH

LH instruction = 020FA

op code = 02

address = 0FA

RH instruction = 210FB

op code = 21

address = 0FB

Since this is in hexadecimal from you have to convert the numbers to binary form.

LH instruction.

02 = 0000010 = Load - M(x)

M(x) refers to the memory address location 0FA.

The first 5 bits of OBC should read -  
Load - M(0FA)

RH instruction.

21 = 0010001 = STOR M(x)

M(x) refers to the memory address location 0FB.

The second 5 bits of OBC should read -  
STOR M(0FB)

Finally the assembly language code for  
OBC 020FA 210FB is

Load - M(0FA)

STOR M(0FB)



B. Explain this program that does.

1. In 08A address the M(OFA) transfer to the accumulator & transfer contents of accumulator to memory location OFB.
2. In 08B address the M(OFA) transfer to the accumulator & take next instruction, from left half of M(08D).
3. In 08C address the M(OFA) transfer to the accumulator & transfer contents of accumulator to memory location OFB.