Name: Mohammad Bilal

ID: 14956

Program: BS(CS)

Instructor: Sir M. Amin

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Q1:
Ans: a

Pipelining: Processor moves data or instructions into a conceptual pipe with all stages of the pipe processing simultaneously.

Branch prediction: Processor looks ahead in the instruction code fetched from memory and predicts which branchs or groups of instructions, are likely to be processed next.

Supersealer execution: This is the ability to issue more than one instruction in every processor clock cycle.

Data flow analysis: Processor analyzee which instruction are dependent on each other's results, or data, to creat an optimized schedule of instruction

Speculative execution: using branch prediction and data flow analysis, some processors speculatively execute instructions ahead of their actual appearance in the program execution.

ans: b

* Deals with the Potential Speedup of a program using multiple Processors Compared to a single Processor.
* Illustrates the Problems facing industry in the development of multi-core machines
* Can be generalized to evaluate and design technical improvement in a computer system

$$\text{Speedup} = \frac{\text{Time to execute Program on a single Processor}}{\text{Time to execute Program on N Parallel Processor}}$$

$$= \frac{T(1-F) + TF}{T(1-F) + \frac{TF}{N}} = \frac{1}{(1-F) + \frac{F}{N}}$$

Ans: C

QPI Protocol Layer: In this layer, the packet is defined as the unit of transfer. The packet contents definition is standardized with some flexibility allowed to meet differing market segment requirements. A typical data packet payload is a block of data being sent to or from a cache.

Ans: D

PCI Physical and Logical Architecture.

A root Complex device, also referred to as a chipset or a host bridge. Connects the processor and memory subsystems to the PCI Express switch fabric comprising one or more PCIe and

PCIe switch devices.

* Switch: The switch manages multiple PCIe streams.

* PCIe endpoint: An I/O device or Controller that implements PCIe such as a Gigabit ethernet switch, a graphics or video Controller, disk interface, or a Communications Controller.

Legacy endpoint: legacy endpoint Category is intended for existing design that have been migrated to PCI Express endpoints are not permitted to require the use of I/O space at runtime and must not use locked transactions.

Q.2

Ans: a

Consequences of Moore's Law

* Higher packing density means shorter electrical paths, giving higher performance
* Smaller size gives increased flexibility
* Reduced power and cooling requirements
* Fewer interconnections increase reliability.

Ans: b

The key characteristics of a computer family are:

* Similar or identical instruction set: In many cases, the exact same set of machine instruction are supported on all members of the family.
* Similar or identical operation system: The same basic operating

system is available for all family members.

* Increasing speed: The rate of instruction execution increases in going from lower to higher family members.

* Increasing of I/O ports: In going from lower to higher family members.

* Increasing memory size: In going from lower to higher family member.

* increasing cost in going from lower to higher family member.

Ans: C

* Instruction fetch (iF) Read instruction from its memory location into the processor.

* Instruction operation decoding (iod) Analyze instruction to determine type of operation to be performed and operand(s) to be used

* Operand address calculation (oac) if the operation involves reference to an operand in memory.

* operand fetch (OF) fetch the operand from memory or read it in from I/O

* Data Operation: (do) Perform the operation indicated in the instruction.

* operand store (OS): write the result into memory or out to I/O

Ans: d

Classes of interrupts

* Program: Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction etc.

* Timer: Generated by timer within processor.

* I/O: Generated by an I/O controller, to signal normal completion of an operation or to signal a variety of error conditions.

* Hardware Failure. Generated by a failure such as Power failure

Q.3

Ans: a

ARM Cortex	Cortex-A
operating system	Higher Performance Rich OS/RTOS
instruction set	32/64 bit ARM & Thumb ISA
Interrupts	SW-managed interrupt
Bus interface	AMBA Axi

ARM Cortex	Cortex-R
operating system	RTOS only
instruction set	Thumb ISA
Interrupts	Deterministic SW-managed
Bus interface	AMBA Axi

Cortex-M : Lower Power, Smaller area.

Operating system: RTOS only

Instruction set: Thumb ISA

Interrupts : HW-managed interrupt

Bus interface: AMBA AHB/AXI

Ans: b

Multicore: The use of multiple processors on the same chip, also referred to as multicore or multicore, provides the potential to increase performance without increasing the clock rate. In addition, with two processors, larger caches are justified.

This is important because the power consumption of memory logic on a chip is much less than that of processing logic.

many integrated core (MIC). The multicore and MIC strategy involves a homogeneous Collection of general purpose processors on a single chip. At the same time, chip manufacturers are purpose processors on a single: a chip with multiple general-purpose processors plus graphics processing units (GPUs) and specialized cores for video processing and other task. In broad terms, a GPU is a core designed to perform parallel operations on graphics data. Since GPUs perform Parallel operation on multiple sets of data, they are increasingly being used as vector for a variety of application that require repetitive computations.

Q: 4

Ans: a

1) ISU (instruction sequence unit): Determines the sequence in which instructions are executed in what is referred to as a superscalar architecture.

2) IFU (instruction fech unit): Logic for fetching instruction.

3) IDU (instruction decode unit): The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

4) LSU (load-store unit): The load contains the 96-KB L1 data cache 1, and manages data traffic between the L2 data cache and the functional execution units.

5) XU (translation unit): This unit translates logical addresses from instructions into physical addresses in main memory.

6) BFU (Binary floating-point unit): The BFU handles all binary and hexadecimal floating-point operations, as well as fixed-point multiplication operations.

7. DFU (decimal floating-point unit): The DFU handles both fixed-point

and floating-point operations on numbers that are stored as decimal digits.

8) RU (recovery unit): The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signal, and manages the hardware recovery actions.

9) COP (dedicated coprocessor): The COP is responsible for data compression and encryption function for each core.

10) I-Cache: This is 64-KB L1 instruction cache, allowing the IFU to prefect instruction before they are needed.

11) L2 Control: This is the control logic that manages the traffic through the two L2 caches.

12) Data_L2: A 1-MB L2 data cache for all memory traffic other than instructions

13) Instr_L2: A 1-MB instruction cache.

Q.5

Ans: A

Clock speed of the processor 60 MHz

Number of instruction the executed program consists: 104000

Calculating the CPI:

The formula to calculate CPI is

$$CPI = \frac{\text{Instruction Count} * \text{Cycles Per Instruction}}{\text{Number of instructions}}$$

$$CPI = \frac{(46000 \times 1) + (33000 \times 2) + (16000 \times 2)}{104000}$$

$$+ \frac{9000 \times 2}{104000}$$

$$= \frac{168000}{104000} = 1.616 \approx$$

$$CPI = 1.616 \approx$$

Calculating MIPS

Processor Time $T = Ic \times CPI \times T$

$$MIPS = \frac{Ic}{T \times 10^6}$$

$$= \frac{Ic}{Ic \times CPI \times T \times 10^6}$$

$$= \frac{1}{CPI \times \frac{1}{f} \times 10^6}$$

$$= \frac{f}{CPI \times 10^6}$$

$$MIPS = \frac{60 \times 10^6}{1.616 \times 10^6}$$

$$= \frac{60}{1.616} = 37.128$$

$$MIPS = 37.128$$

Calculating Execution Time(T)

$$T = Ic \times CPI \times \frac{1}{F}$$

$$T = \frac{100000 \times 1.616}{60 \times 10^6}$$

$$= \frac{161600}{6000000}$$

$$= 0.2693 \approx$$

$$\boxed{T = 0.2693^{ms} \approx}$$